Fabricating and Studying van der Waals Heterostructures

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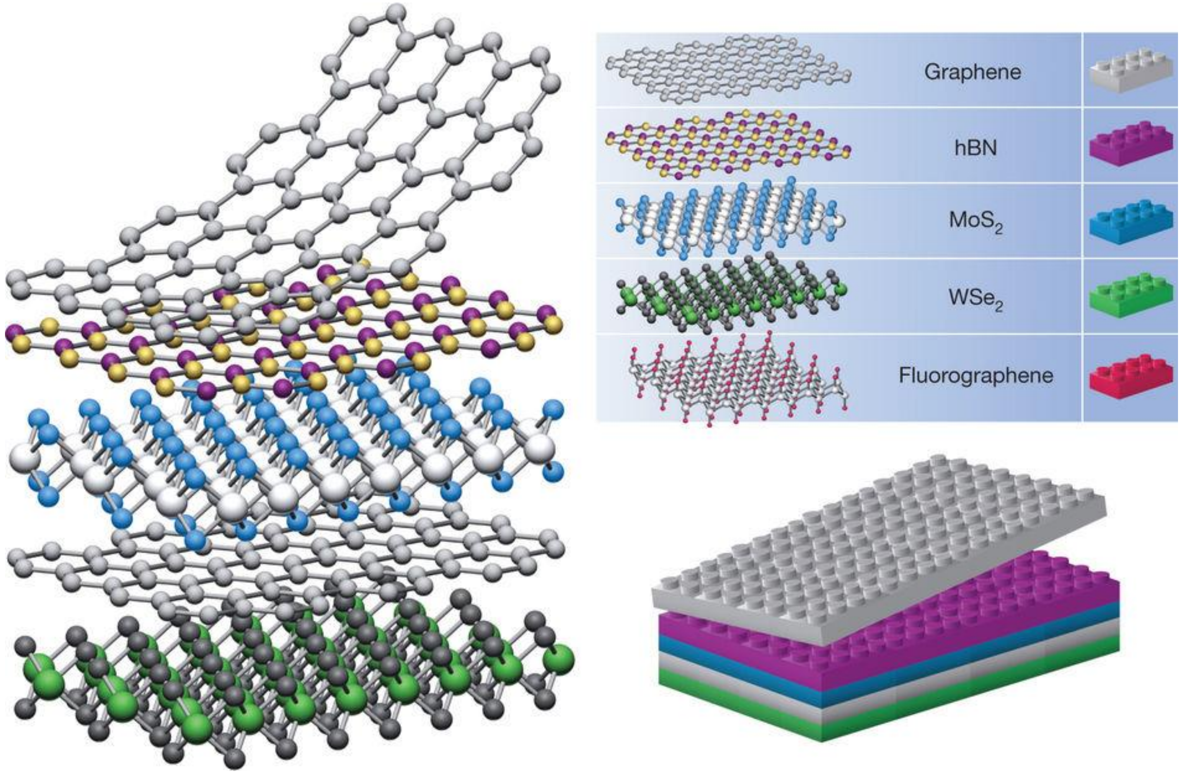
Why van der Waals heterostructures?

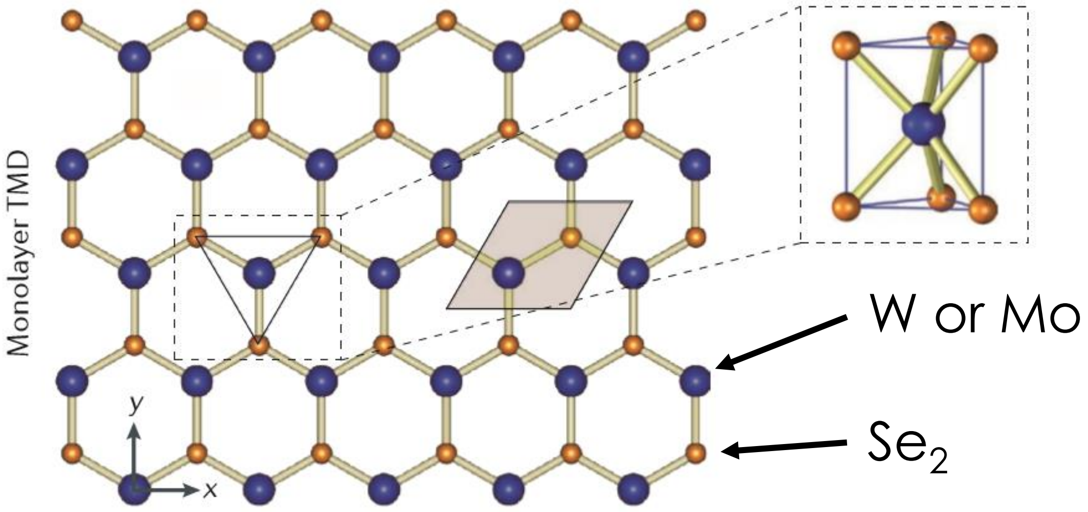
- Lab studies interaction between light, matter, and electric and magnetic fields
- Can stack layers of material to create **van der Waals heterostructures** to observe new physics
- High **degree of control** (electric, magnetic, mechanical) over sample
- **Surface effects** dominate
- Can study bilayer versions of ubiquitous systems such as p-n junctions



Geim & Grigorieva, *Nature*, 2013

Transition metal dichalcogenides (TMDs)

- Hexagonal crystal lattice with chemical formula MX_2



Schaibley et al., Nature Reviews: Materials, 2016

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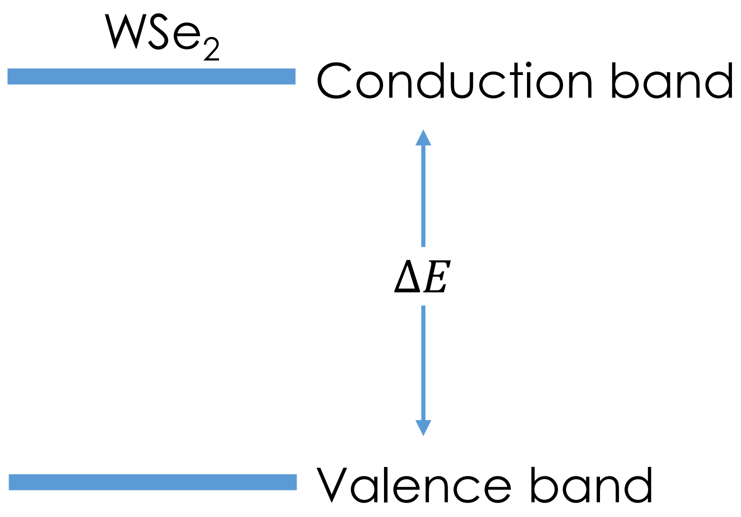
- **Semiconductor** with gap between valence band and conduction band
- Monolayers have **direct bandgap in visible spectrum ➔** strong absorption and emission



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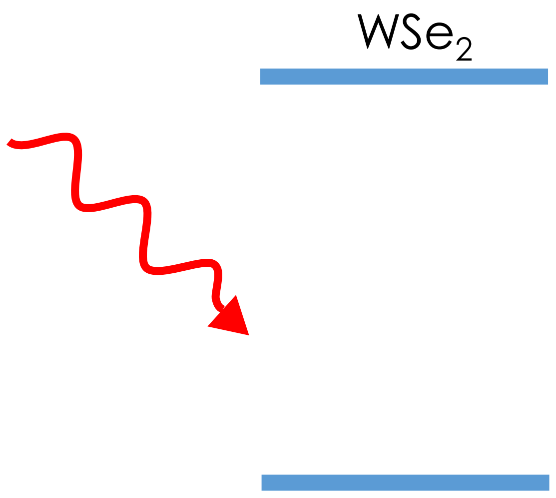

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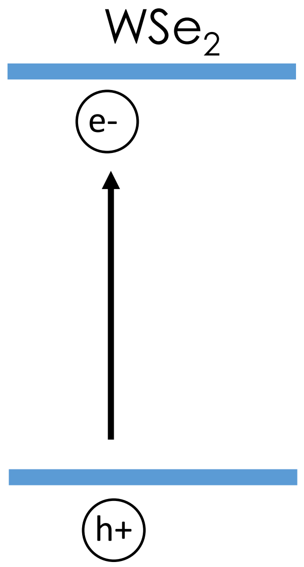

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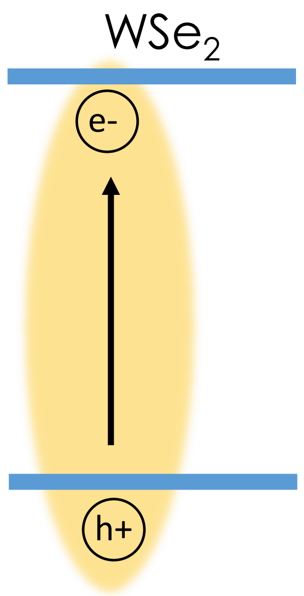

Bound electron-hole **exciton**

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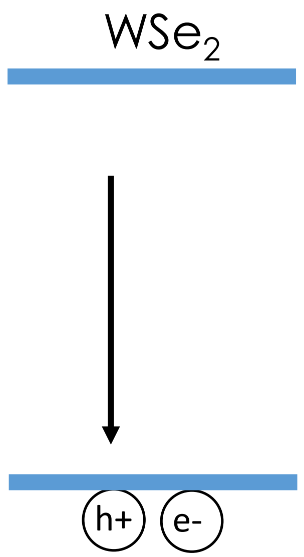

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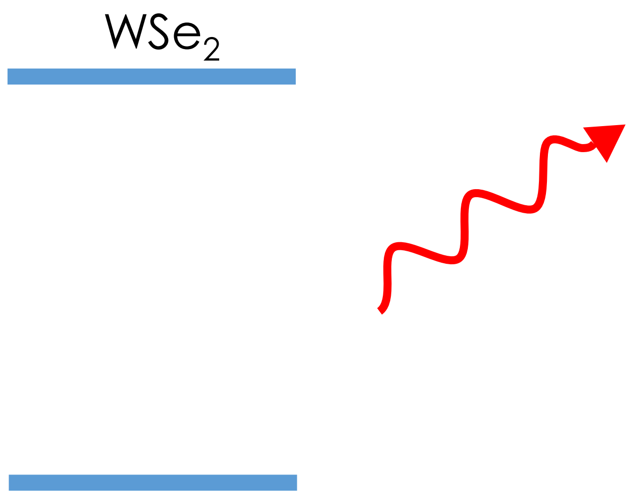

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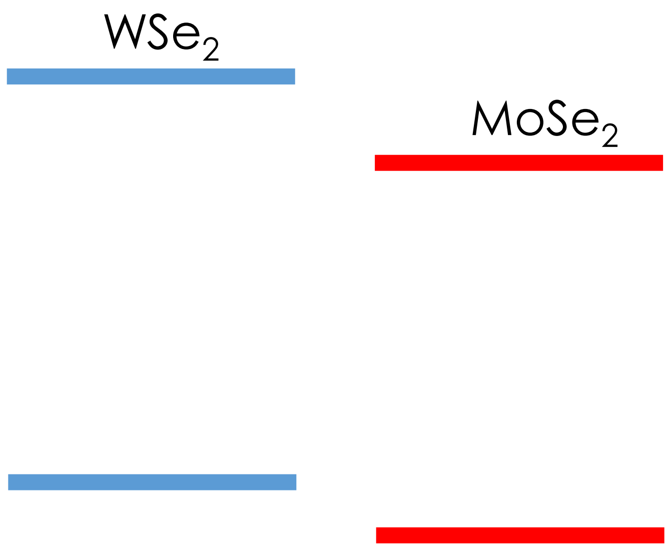

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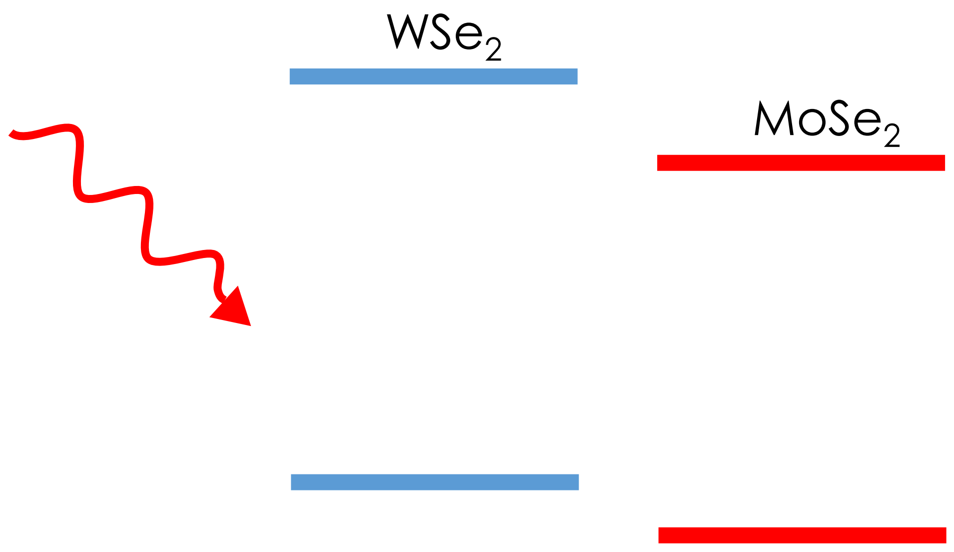

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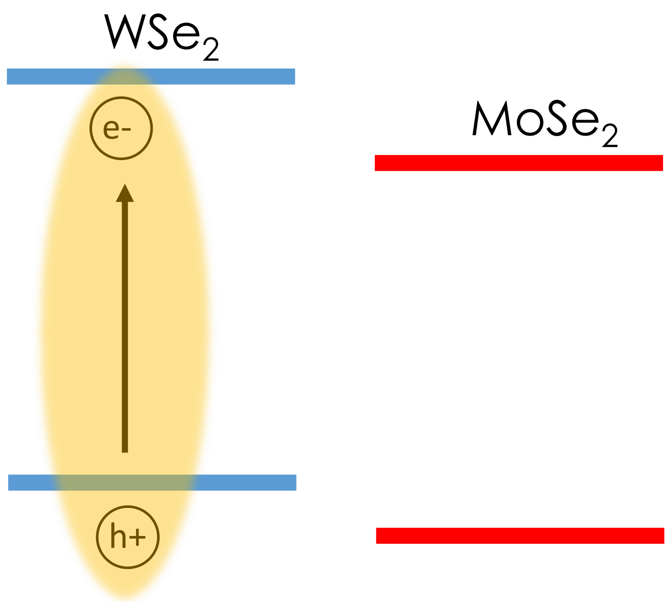

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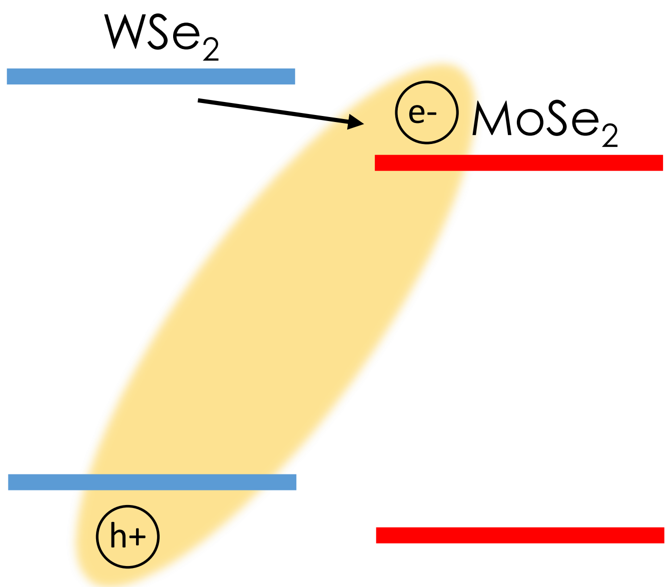
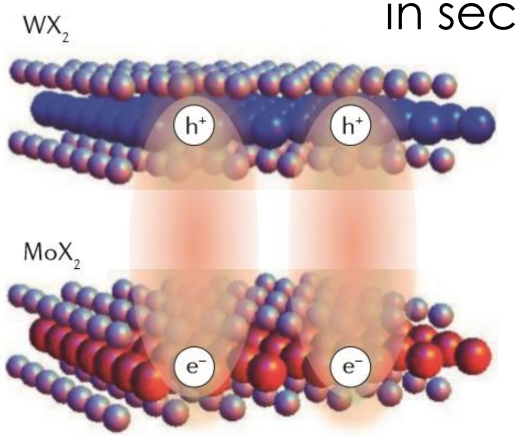


electron moves to lower energy in second material



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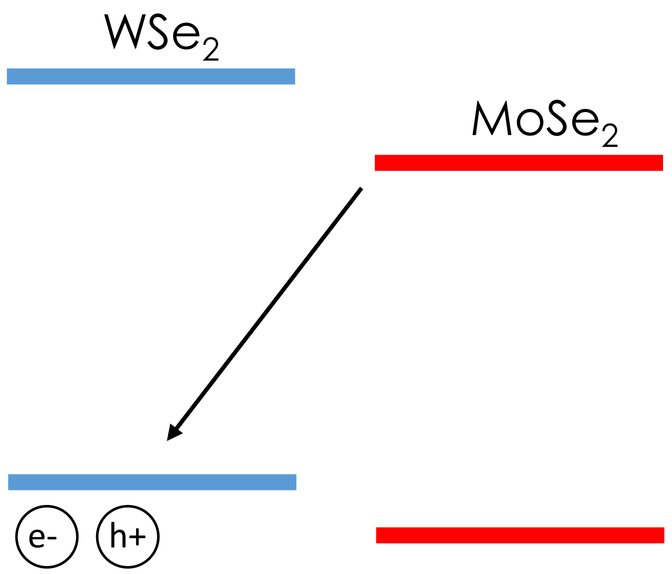

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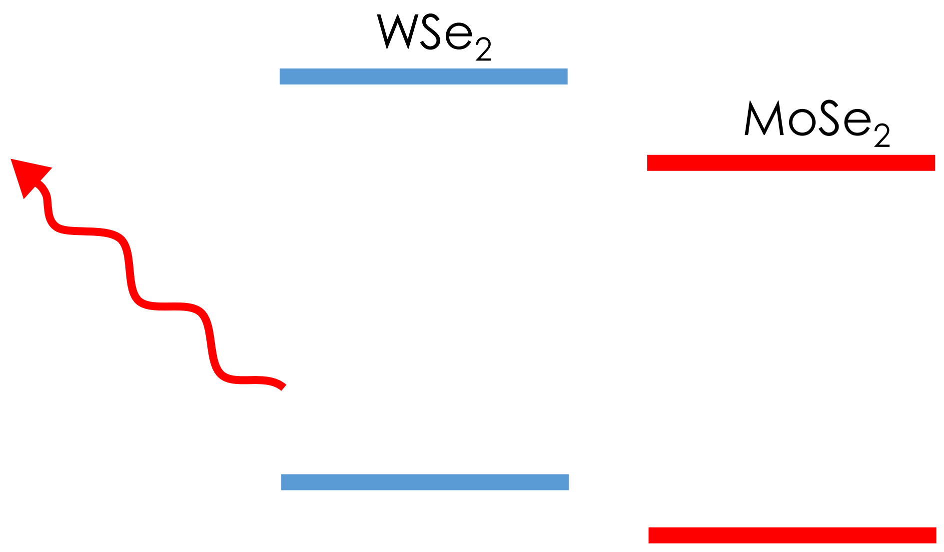
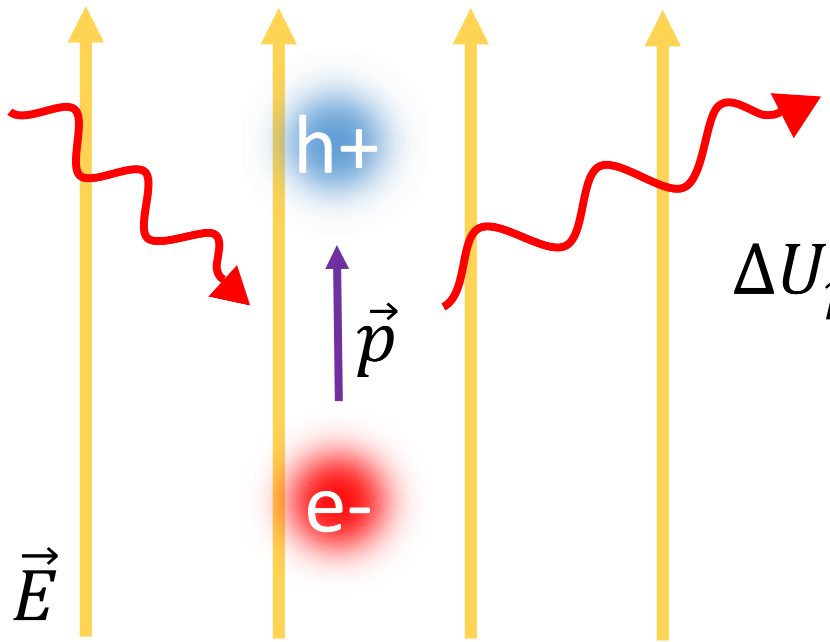


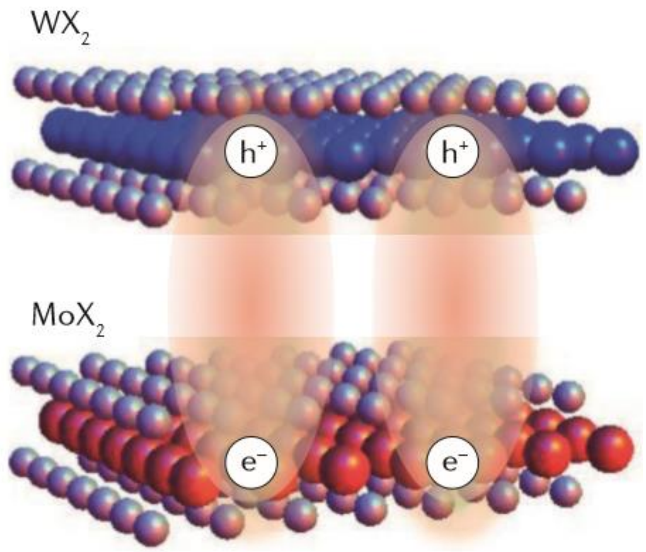
Studying interlayer excitons

- Applied electric field reveals **quantum-confined Stark effect**
- Want to measure exciton **decay time** and **energy emission spectrum** as a function of the applied electric field



$$\Delta U_{photon} = -\vec{p} \cdot \vec{E}$$

Schaibley et al., Nature Reviews: Materials, 2016



Seeing the physics: device to data

- Idea for device

→

- Find materials
- Ensure quality
- Characterize

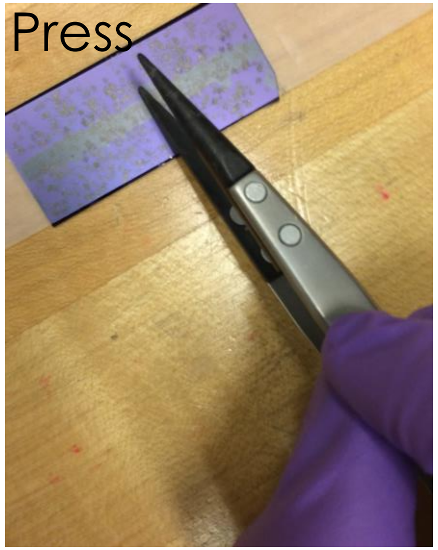
→

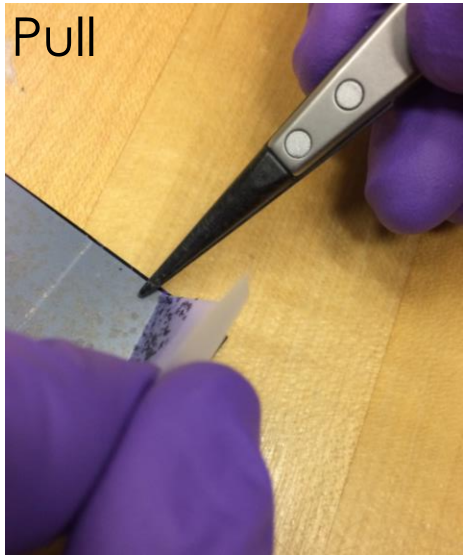
- Design device
- Stack pieces
- Make electrical contact
- Wire electrical contacts to cryostat

→

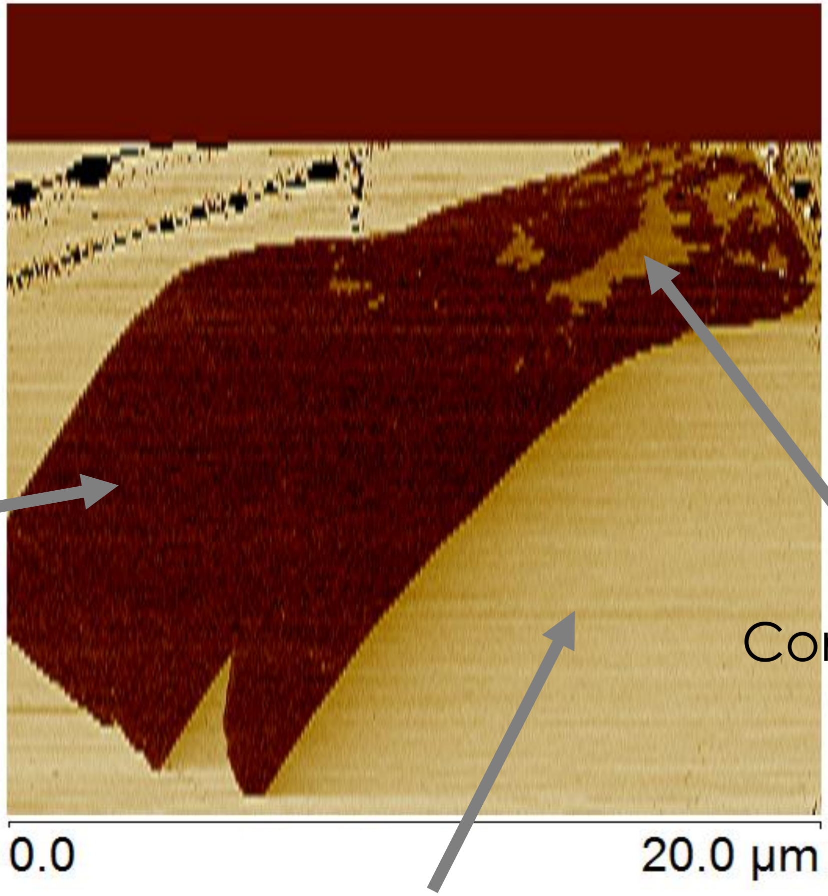
- Cool to T < 4K
- Collect data
- Discover interesting new physics?

Fabrication Process: Collecting Materials





Atomic force microscopy further resolves distances and reveals cleanliness



Flake of $MoSe_2$

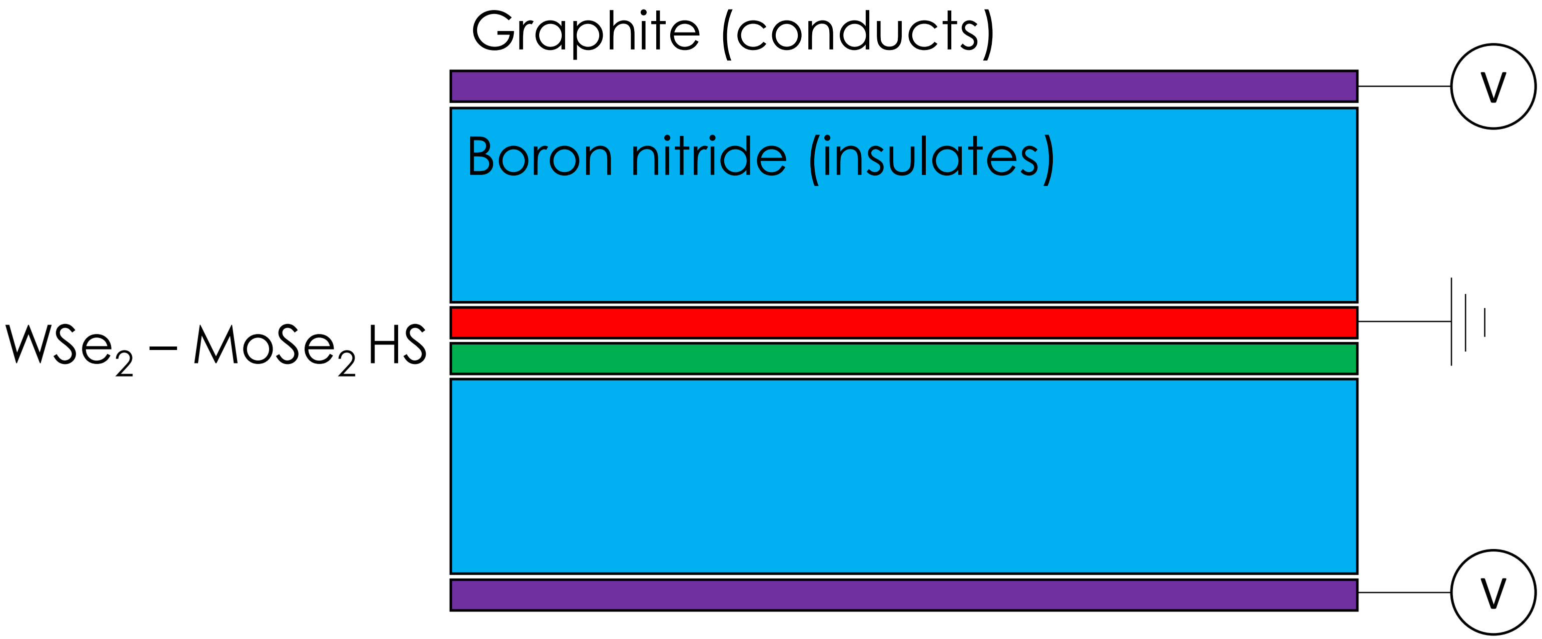
Contaminant

Silicon chip

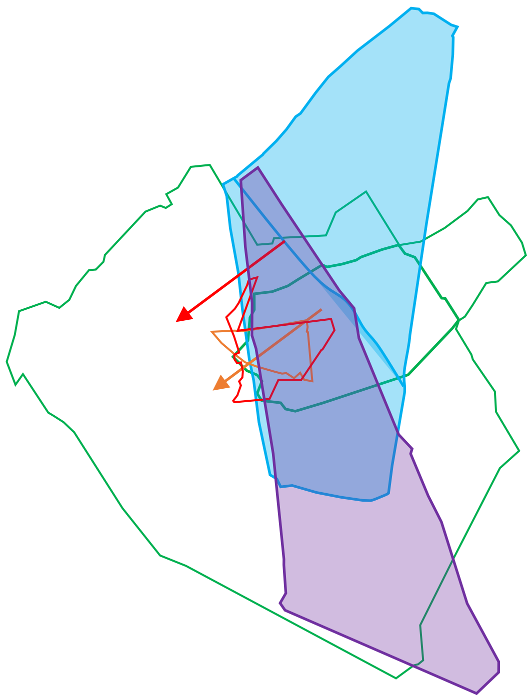
Fabrication Process: Device Planning

Or, “measure twice, cut once”

Desired electrical control dictates stacking pattern

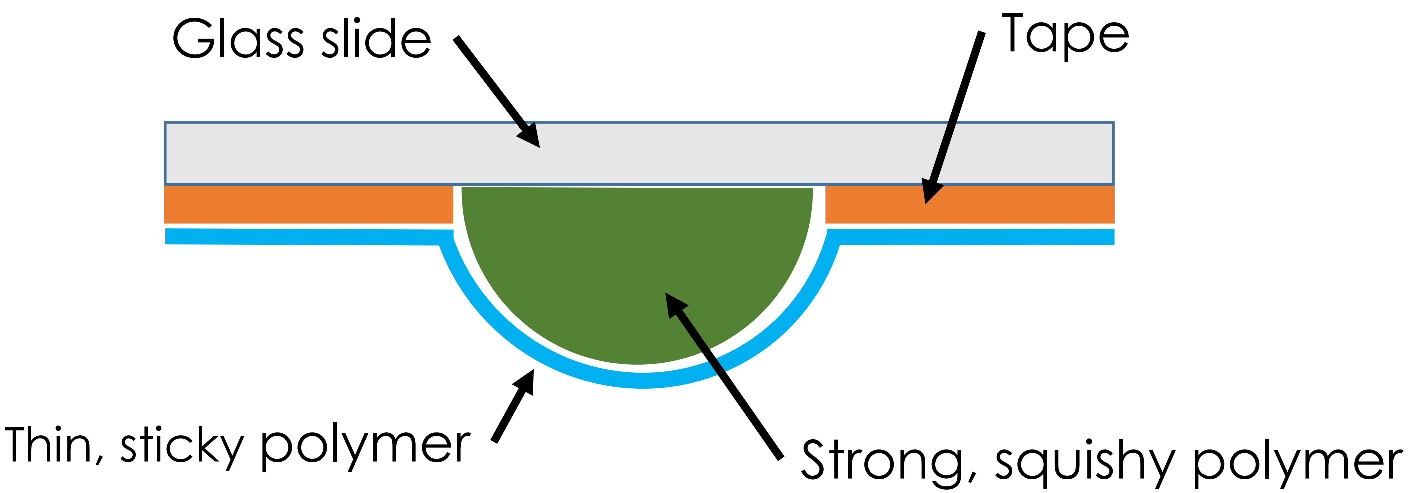


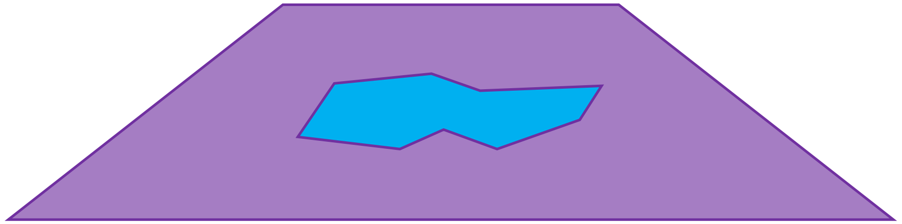
Need to know precise orientation and where to pick up each piece



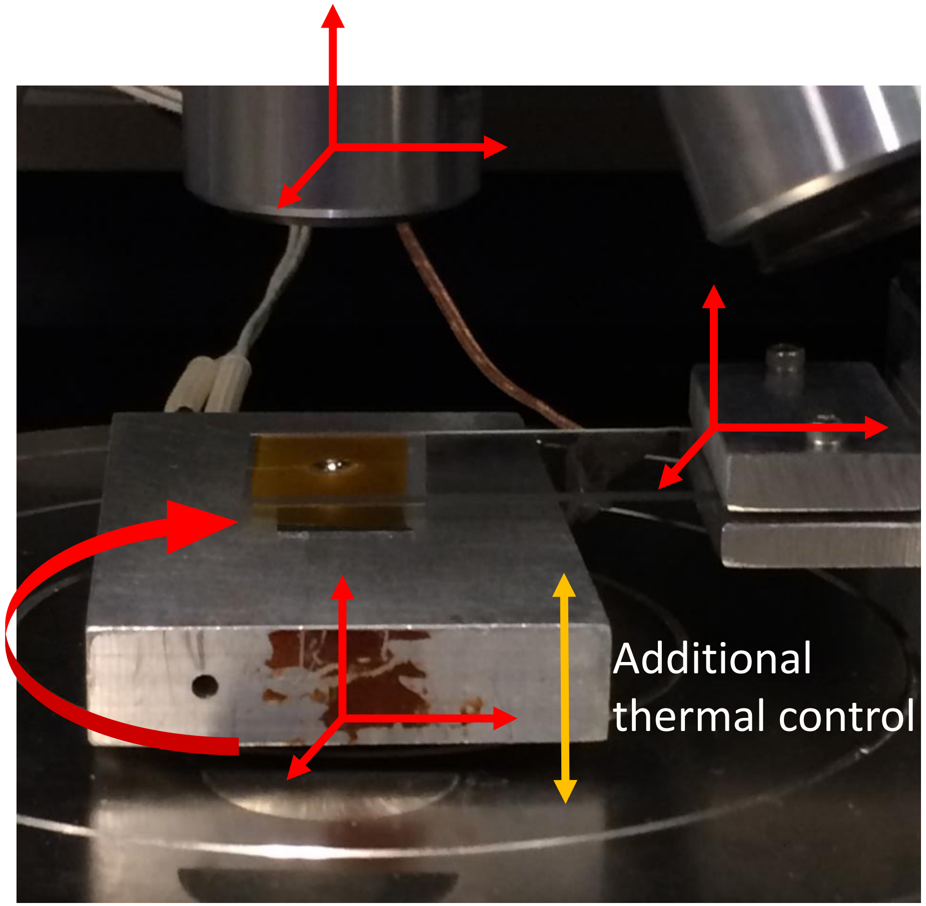
Fabrication Process: Transfer

Stamp





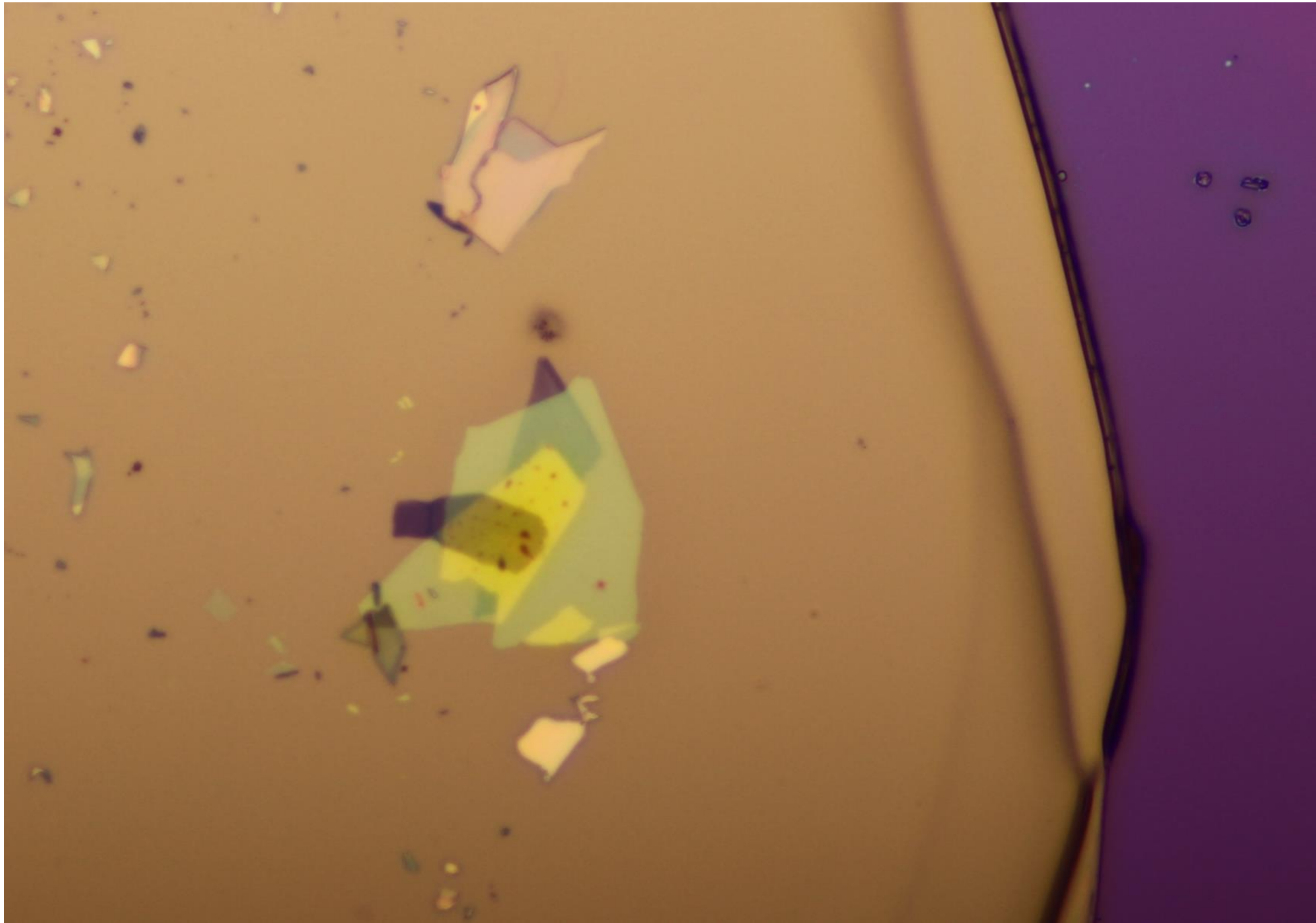
Si chip with target sample



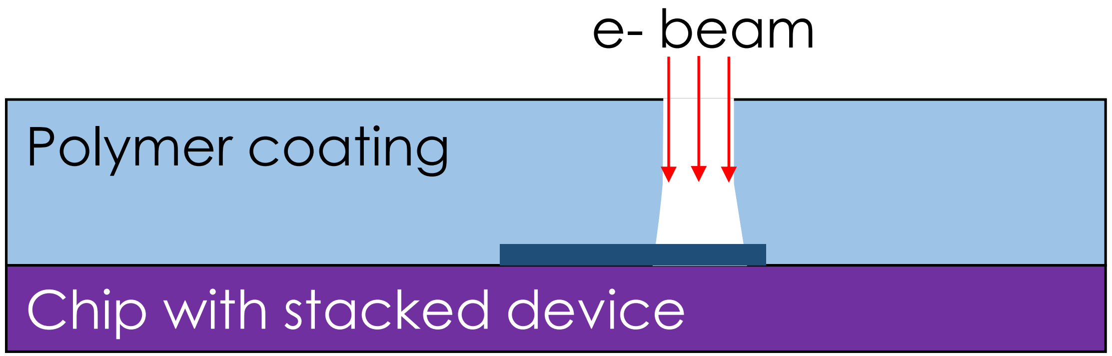
<u>many</u> degrees of freedom

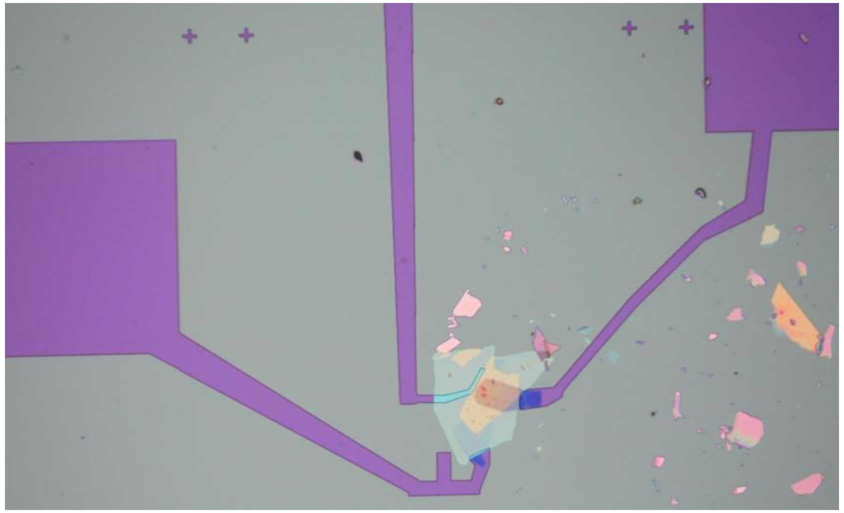
Fabrication Process: Transfer

Melting down stamp covering assembled device onto chip



Fabrication Process: Evaporating Contacts





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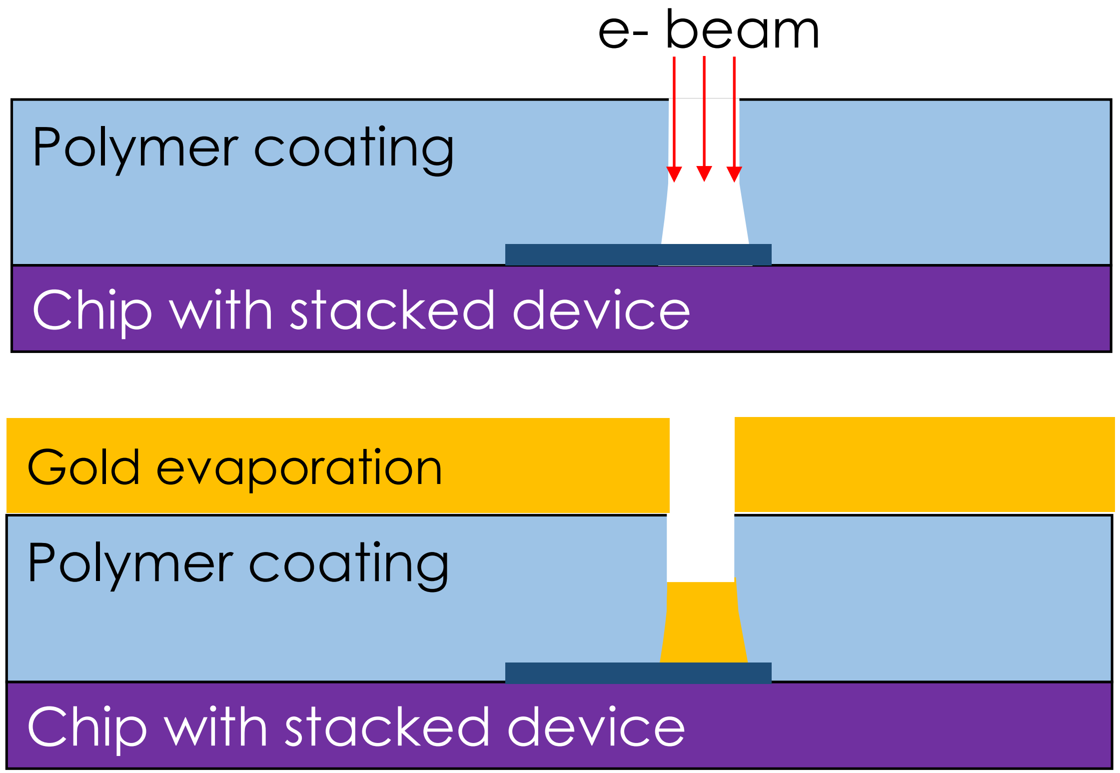

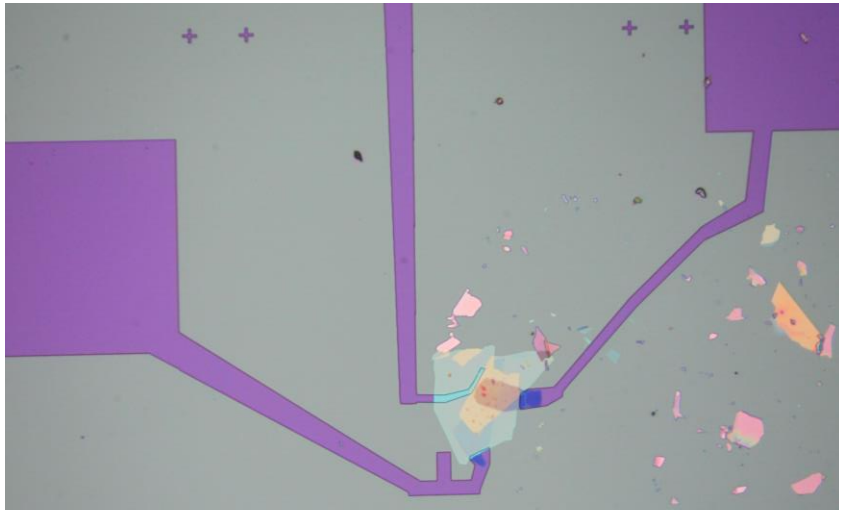

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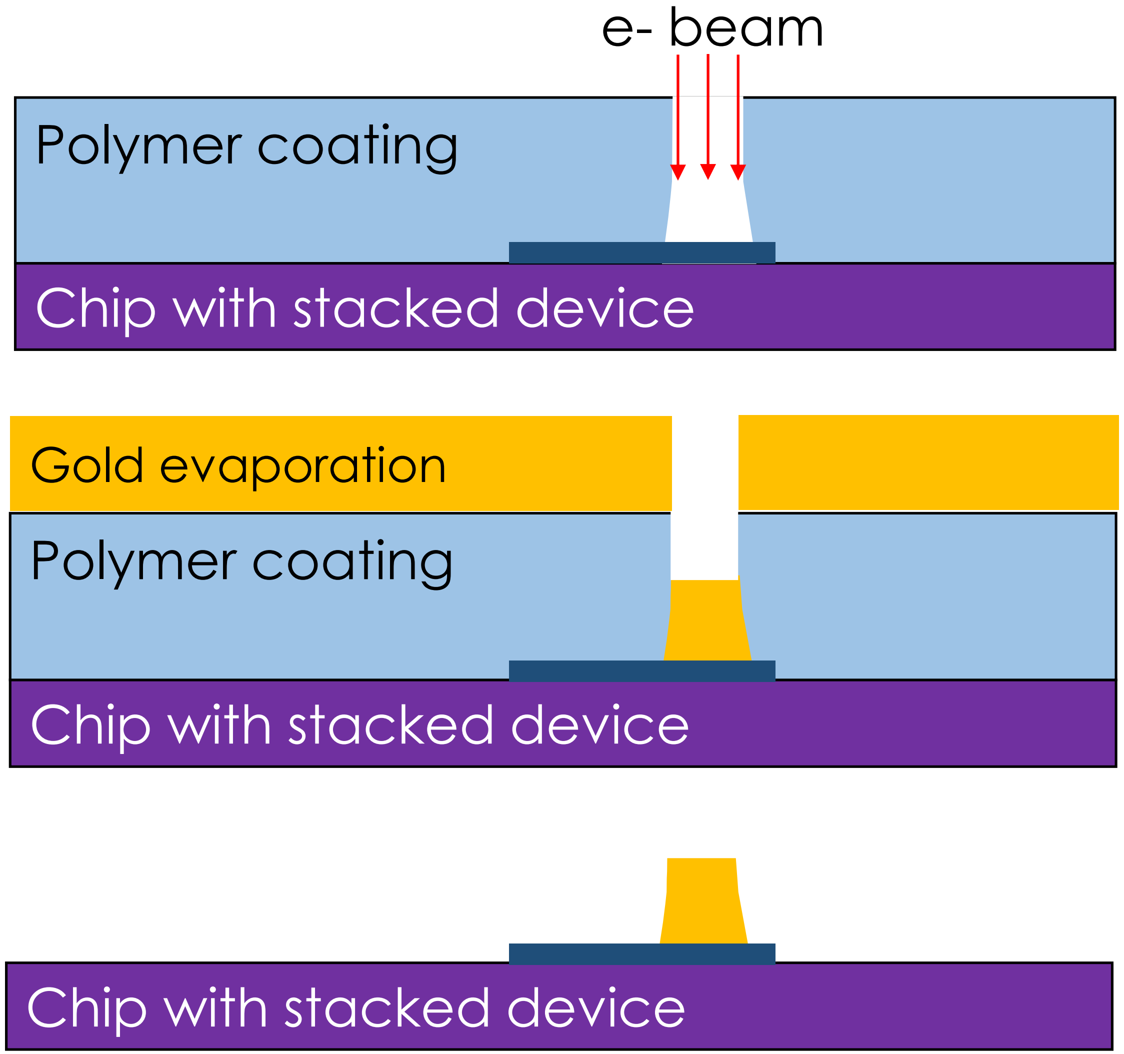
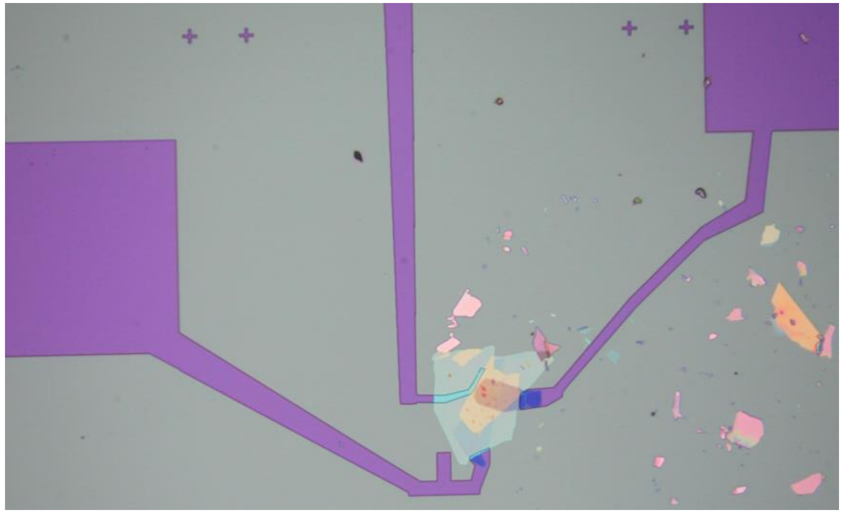
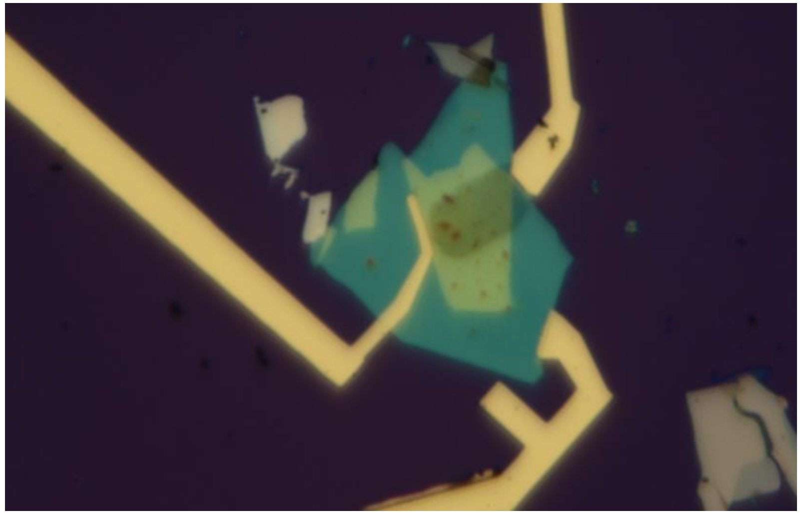
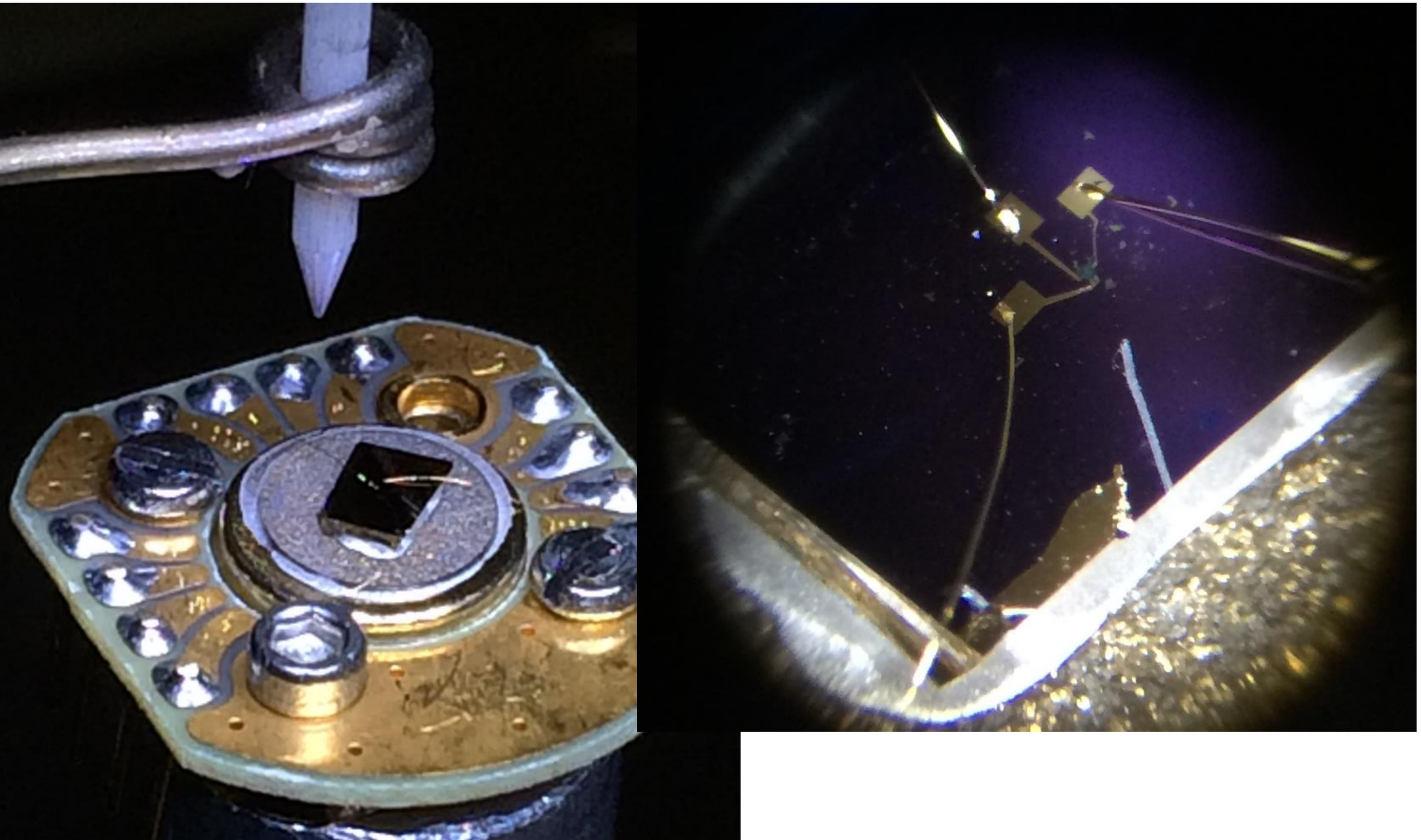






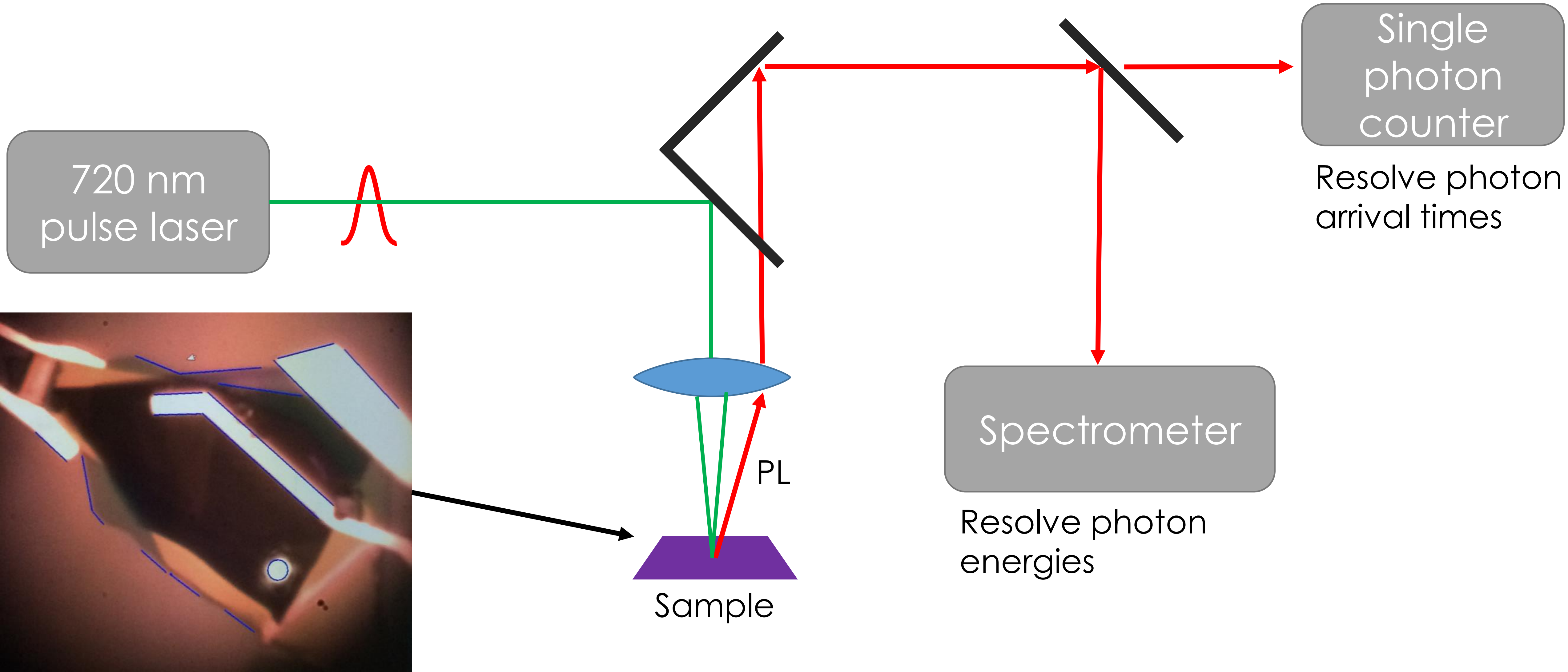
Fabrication Process: Wire-bonding & Cooldown

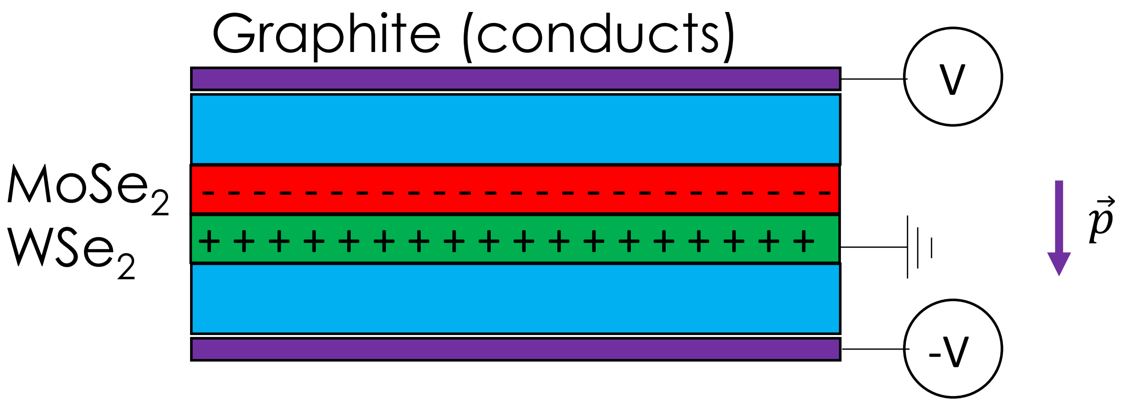
Wiring electrical contact (gold) between device and mount



Completed device in cryostat

Data Collection: Experimental Schematic





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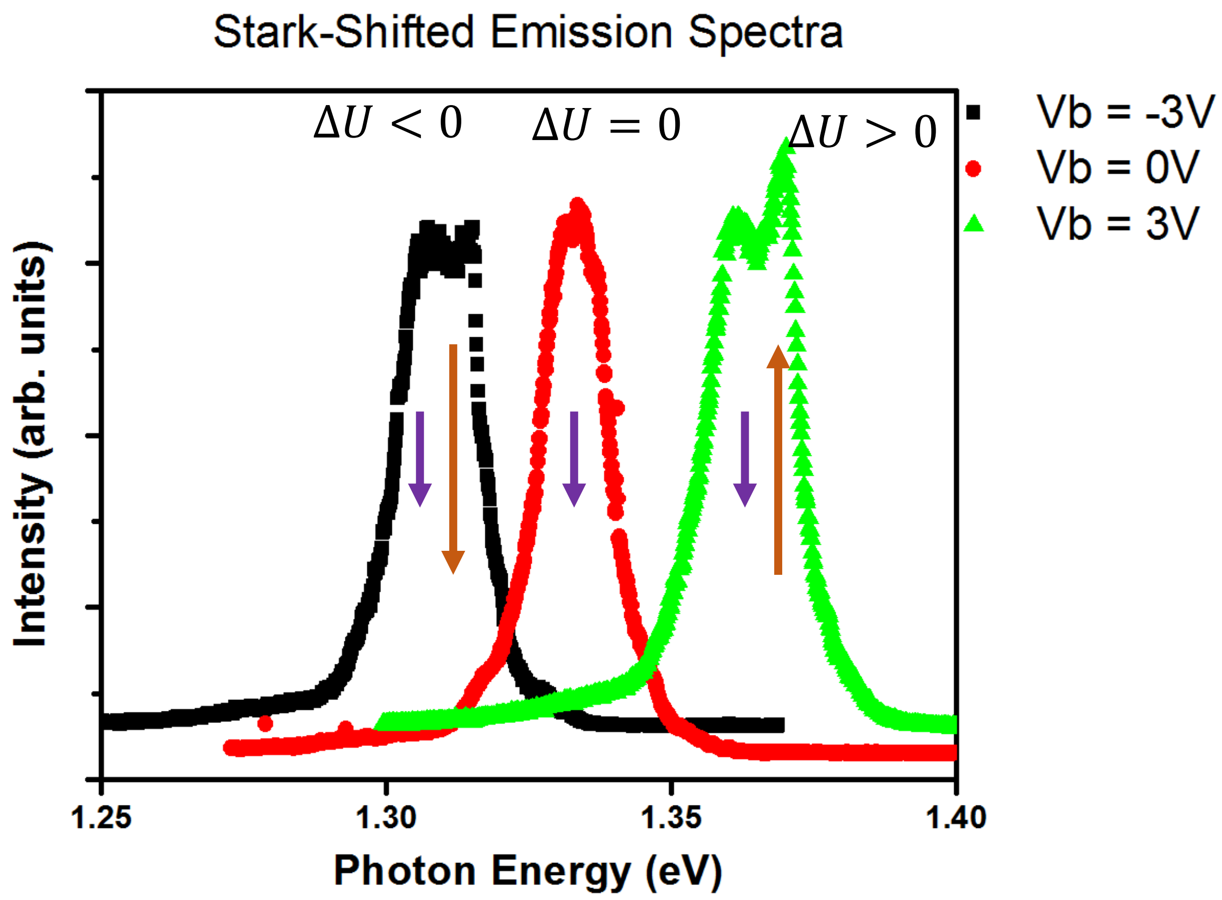

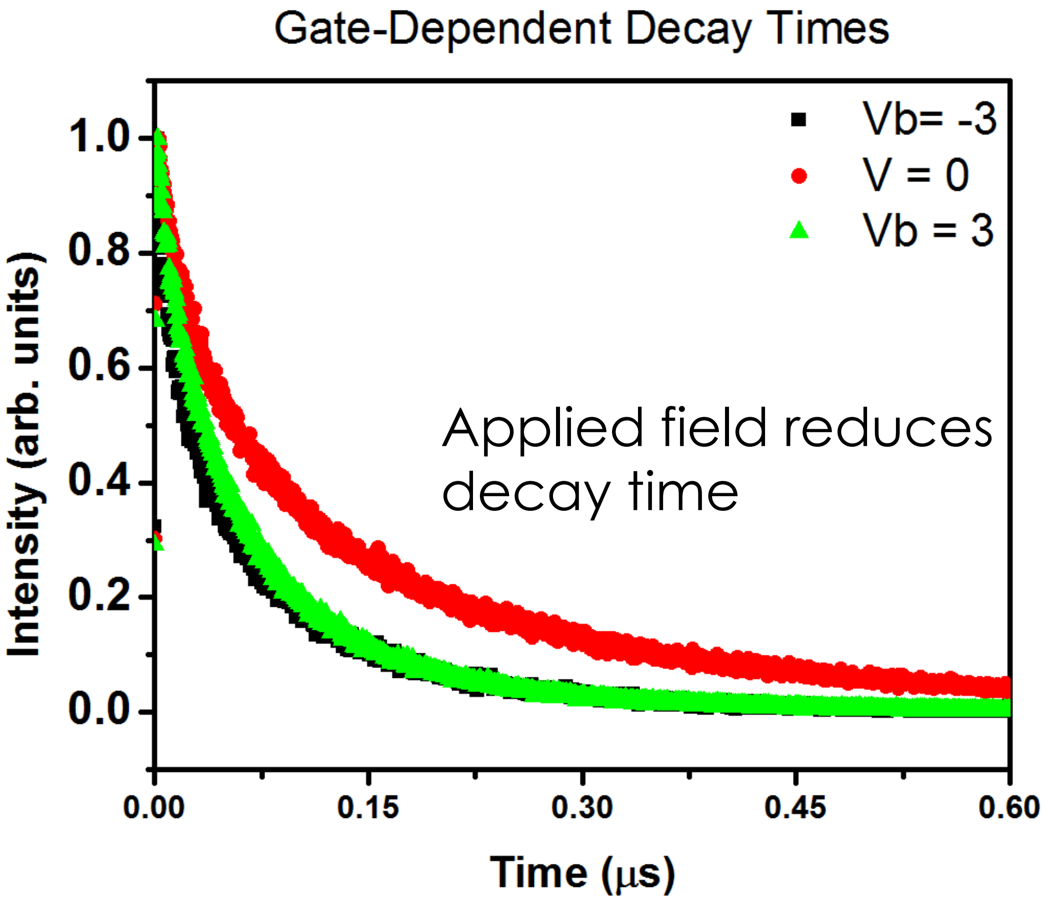

What it means; where its going

- Discovering new physical phenomena
- Applications to photon energy harvesting, information technology and perhaps more
- Assembly and mass-production are difficult
- Not all the observed effects are understood, and not all the predicted effects have been observed
- “Publish or perish” ➔ “Device or doom”

Acknowledgements

- The NSF REU program and the University of Washington
- Professor Xiaodong Xu for hosting me in the lab
- Pasqual Rivera for mentoring me
- The Xu group for answering questions and supporting my work, especially Nathan and Gen for taking time to help me with my project

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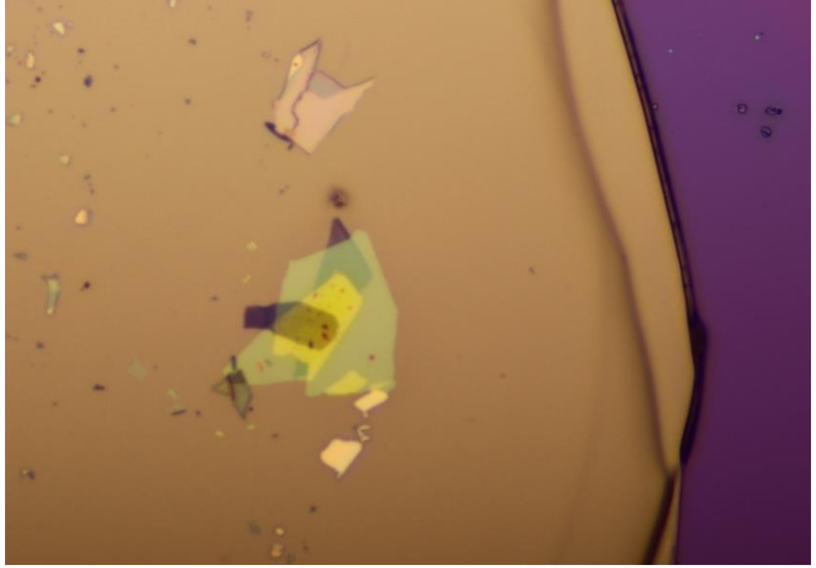
References

[1] A. K. Geim and I. V. Grigorieva, "Van der Waals Heterostructures," *Nature*, vol. 499, pp. 419 – 425, 2013.

[2] J. R. Schaibley, H. Yu, G. Clark, P. Rivera, J. S. Ross, K. L. Syler, W. Yao and X. Xu, "Valleytronics in 2D materials," *Nature Reviews: Materials*, vol. 1, pp. 1-15, 2016.

[3] X. Xu, W. Yao, D. Xiao and T. F. Heinz, "Spin and pseudospins in layered transition metal dichalcogenides," *Nature Physics*, vol. 10, pp. 343-350, 2014.

Fabrication Process: Transfer



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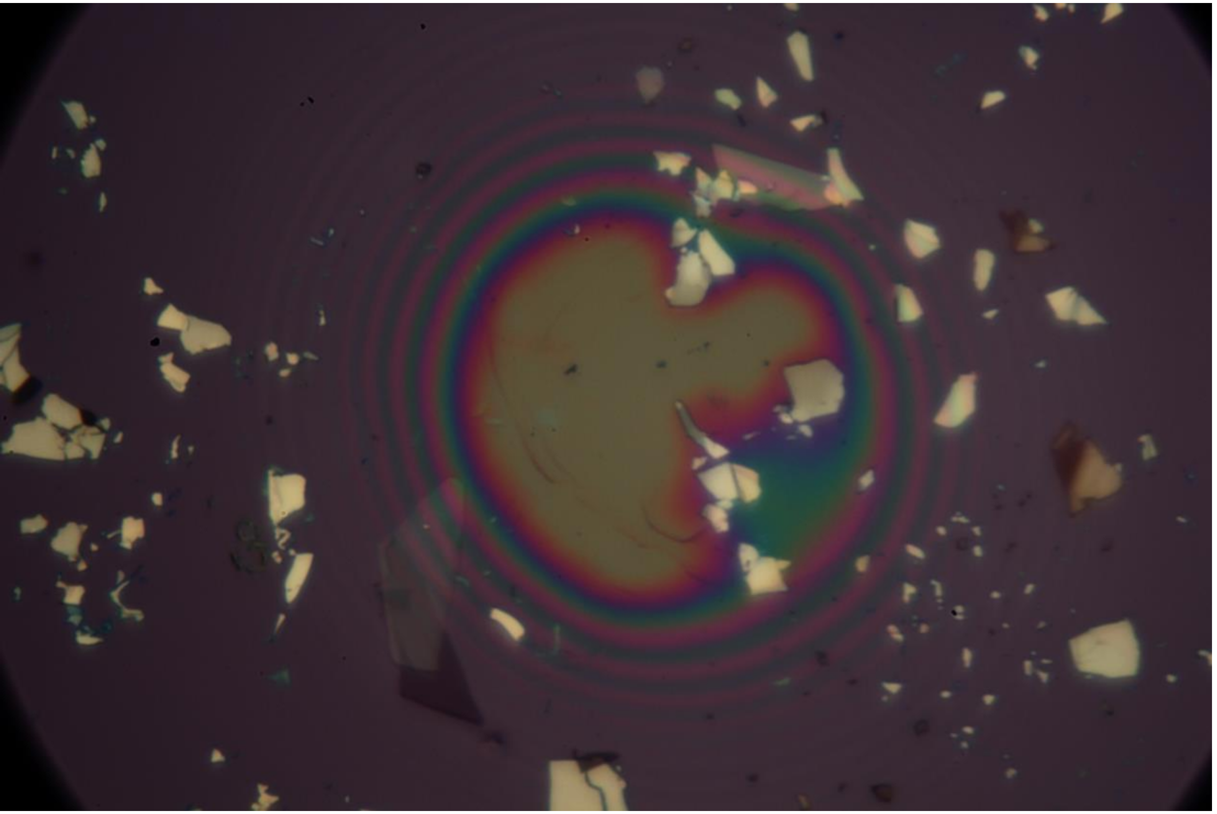

Lifting piece off of chip

Full transfer station