Fabricating and Studying van der Waals Heterostructures

Jordan Fonseca*
Department of Physics, University of Puget Sound

PI: Xiaodong Xu
Graduate Student Mentor: Pasqual Rivera
University of Washington

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As methods for fabricating and studying van der Waals heterostructures (HS) become more sophisticated and established, solid-state physicists are reliably able to probe exotic and novel physics in the 2D limit. Monolayer transition metal dichalcogenides (TMDs) are semiconductors with a direct bandgap. When two different monolayer TMDs, WSe_2 and $MoSe_2$, are stacked to create a van der Waals heterostructure, the slightly offset band structures of the two materials forms a system with type-II band alignment (p-n junction). Assembling these van der Waals HS devices requires a sophisticated fabrication process, which contributes the bulk of this report. By electrostatically gating the HS to apply an electric field of variable strength, we demonstrate the quantum-confined Stark effect in this 2D system with a shift in exciton dipole energy of approximately 0.06 eV as the potential difference across the HS is swept from -6V to 6V. In addition to the exciton energy dependence on the electric field, we report a change in 1/e decay time of the state of the interlayer exciton from roughly 100 ns in the absence of an electric field to roughly 50 ns when a potential difference of ±6V is applied across the HS.

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I. INTRODUCTION

The discovery of monolayer graphite, or graphene [1] opened up the now-prominent field of two-dimensional (2D) materials within solid state physics. With the advent of additional 2D materials, such as the transition metal dichalcogenides (TMDs), and the ability to stack these materials into van der Waals heterostructures [2], the opportunities to study a host of new physical properties abound. In this paper, we discuss a narrow but exciting subset of the field: TMD van der Waals heterobilayers, referring to layers of different materials (in this case, TMDs) held together by weak van der Waals interaction. In the broadest terms, van der Waals heterostructure devices are interesting because they facilitate the study of new physics that arises when single layers of distinct materials are stacked together and subjected to external fields. In some cases, these 2D systems are analogous to long-studied and well-understood 3D systems; for example, TMD heterobilayers form a 2D p-n junction, a system ubiquitous in semiconductor physics.

TMDs have the stoichiometry MX_2, where M is a transition metal and X is a chalcogen atom. For our purposes, M will always be tungsten (W) or molybdenum (Mo), while X will be selenium (Se). The TMDs we will discuss are semiconductors with a hexagonal crystal lattice (Figure 1a), and in monolayer form they have a direct bandgap in the visible spectrum at the ±K points of the Brillouin zone. For a more comprehensive and detailed review of TMD physics, see Xu et al.[3]. Vertically stacking two different monolayer TMDs into a heterobilayer (also referred to as heterostructure, or HS) creates a system with type-II band alignment [4], as shown in Figure 1b. This band alignment, more commonly known as a p-n junction in semiconductor physics, gives rise to an exotic phenomenon that will be the focus of this research: the interlayer exciton.

Since monolayer TMDs have a direct bandgap in the visible spectrum, they can efficiently absorb visible photons by promoting a valence electron to the conduction band. When an electron is excited into the conduction band, the previously neutral region it leaves behind is positively charged, which can be considered to be a positively charged quasiparticle known as a hole. The Coulomb attraction between the electron and the hole creates a bound state known as an exciton, another quasiparticle ubiquitous in solid-state physics. In a monolayer, the exciton annihilates after a short ∼ps time [5], emitting a photon in the visible spectrum.

In heterobilayer TMDs, however, an additional transition takes place. If a visible photon excites an electron in WSe_2, the electron can undergo rapid interlayer charge transfer, moving to the lower energy conduction band in the $MoSe_2$ [4]. This energetically favorable transition creates an *interlayer exciton* since the electron and hole comprising the bound state are confined to separate layers in the system (see Figure 1c). Notably, if the inci-

* Correspondence: jfonseca@pugetsound.edu

dent photon is instead resonant with the $MoSe_2$ bandgap, the hole undergoes rapid interlayer charge transfer to its lower energy sate in the WSe_2 valence band. This means that the $MoSe_2$ will always be n-type doped and the WSe_2 will always be p-type doped, as suggested by Figure 1(b,c).

Interlayer excitons are our primary interest, and in particular we present a preliminary analysis of the dependence of the energy and decay time of the exciton on an out-of-plane, external electric field. By measuring the energy shift in the exciton emission spectrum as a function of the electric field, we can roughly estimate the interlayer spacing between $MoSe_2$ and WSe_2 and compare our result to first-principles calculations.

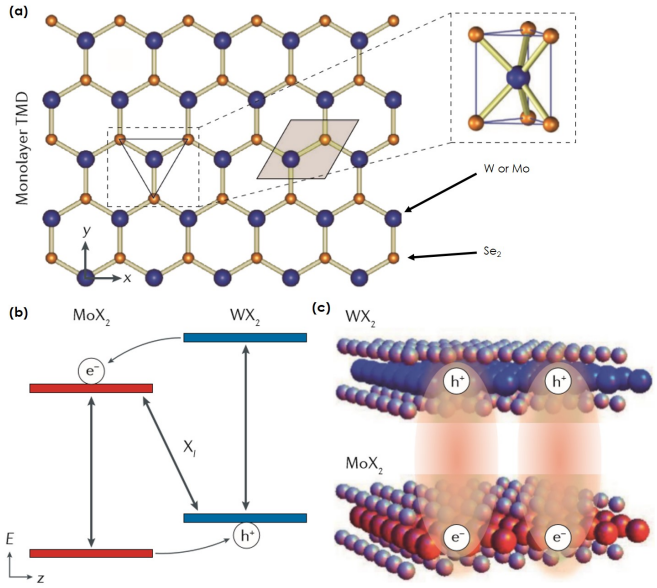

FIG. 1. **(a)** Top-down and side view of crystal structure of monolayer MX_2. **(b)** Type-II band alignment of $MoSe_2$-WSe_2 heterobilayer showing how rapid interlayer charge transfer of conduction band electrons from WSe_2 to $MoSe_2$ or of valence band holes from $MoSe_2$ to WSe_2 produces p-type doping in WSe_2 and n-type doping in $MoSe_2$. **(c)** Schematic showing how p-type and n-type doping of monolayers in a heterobilayer produce spatially separated interlayer excitons. All subfigures adapted from [4].

Although excitons are quasiparticles, the interlayer exciton has an electric dipole moment—equal and opposite charges separated by the distance between the monolayers. In an external electric field, this dipole has a potential energy shift

$$\Delta U = -\boldsymbol{p} \cdot \boldsymbol{E} \tag{1}$$

where $\boldsymbol{p}$ is the exciton dipole moment and $\boldsymbol{E}$ is the applied electric field. This energy shift is known as the quantum-confined Stark effect since the electron and hole are confined to their respective monolayers. We can directly observe the change in the exciton energy by studying how the photoluminescence (PL) emission spectrum changes as a function of the applied field.

While a cursory overview of the sought-after physics is straightforward, the fabrication process of assembling a van der Waals heterostructure that allows for control of the electric field is nontrivial and merits a more thorough discussion.

II. FABRICATION METHODS

A. Scotch-tape exfoliation

Device fabrication begins with Scotch tape exfoliation, which is used to generate layers of material of the appropriate dimensions for use in the desired device. First, bulk flakes of material (graphite, boron-nitride, or MX_2) approximately 1 mm in diameter are placed onto the sticky side of a piece of Scotch tape. Next, the tape is folded together and pulled apart 3-5 times, which cleaves the flakes and spreads the material over the surface of the tape, as in Figure 2a. The bulk crystals used in exfoliation should have large regions where a single crystal lattice geometry persists to minimize fault lines between domains within the crystal. Additionally, the material should be high-purity to guarantee minimal inhomogeneity, especially in the MX_2 monolayers. After spreading crystals around the tape, the tape is applied to a silicon (Si) wafer with insulating SiO_2 thermally grown on top. The tape is gently pressed into the wafer (plastic-tipped tweezers work well) to maximize contact between the material flakes and the wafer substrate (Figure 2b). The SiO_2 coating (90 nm or 285 nm thickness) makes thin flakes of the exfoliated material more visible under an optical microscope via thin-film interference.

The exfoliation procedure offering highest yield varies by material and technique. For example, it is well-established that (1) cleaning the Si wafers in an oxygen plasma treatment immediately prior to depositing the material on the wafer and (2) heating the wafer after the tape has been applied but before the tape is peeled away significantly improves quality and quantity of both graphite and MX_2 [6]; however, these approaches reduce the quality of hexagonal boron nitride (h-BN) exfoliation for unknown reasons. Furthermore, wafer heating temperatures and time varies from 120 °C and 135 °C and from one to two minutes, respectively. After the Si chip has cooled, the tape is peeled away (Figure 2c), completing the exfoliation. The chips are searched under an optical microscope (Figure 2d), and flakes of the desired thickness, size, and cleanliness are photographed and marked for later use. Since the thickness of a given flake of material can only be inferred by its color under an optical microscope, it is advisable to use an atomic force microscope to more precisely characterize the thickness of each flake before assembling a device. Even more importantly, atomic force microscopy can reveal contaminants on the surface of a flake that were invisible under an optical microscope, as shown in Figure 2e.

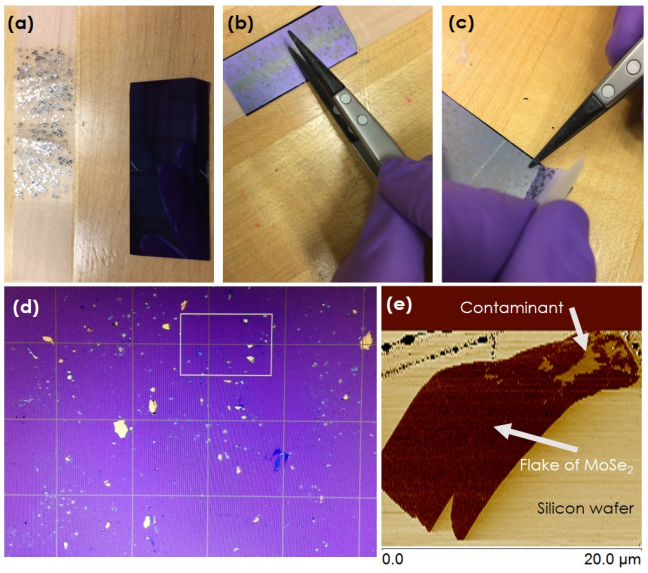

FIG. 2. **(a)** Cleaved and spread graphite flakes on scotch tape next to Si wafer coated with 285 nm of SiO_2. **(b)** Gently pressing tape onto wafer with plastic-tipped tweezers. **(c)** After heating the wafer with tape adhered and letting the chip cool, the tape is slowly peeled away, leaving some exfoliated material behind. **(d)** The chip must be searched under and optical microscope for pieces of the right color (which indicates thickness), size, and cleanliness. If desirable flake are found, they can be photographed and recorded for later use. **(e)** Image of flake of $MoSe_2$ monolayer taken with atomic force microscope to reveal contaminants that were invisible even under a high-magnification (100X zoom) optical microscope. AFM measurements can also precisely determine flake thickness, but this is unnecessary for a monolayer.

B. Device Design

After collecting flakes of material and ensuring their quality, the concept for a device must be reconciled with the shape and size of the available flakes of material. Oftentimes, the desired electrical control greatly constrains how the pieces can be stacked, as is the case for the type of device presented here. In particular, to sustain and control an an out-of-plane, uniform electric field over the heterostructure without transferring charge onto the bilayer, the capacitor-like schematic depicted in Figure 3a was chosen. Electrical gating of the HS is achieved by two flakes of conducting graphite, separated from each other by ∼60 nm of dielectric BN and independently gated.

Since the top and bottom gates can be separately charged, and because the HS itself is grounded, this device allows for control of the electric field strength. When the graphite potentials are set to opposite magnitudes, the device resembles a capacitor with equal but opposite charges producing an electric field perpendicular to the HS surface that can be varied in strength.

It is straightforward to see how the desired electrical control constrains the ways in which the flakes of material can be stacked. Figure 3b shows a schematic of how pieces of the depicted shapes were stacked with these constraints in mind. Note that the top and bottom graphite pieces extend over the HS to enable gating but are always separated from each other by both pieces of BN to prevent charge from shorting from either graphite to the HS or from one piece of graphite to the other. Furthermore, the graphite gates and the HS extend beyond the BN so that the necessary electrical contact can be made with each component.

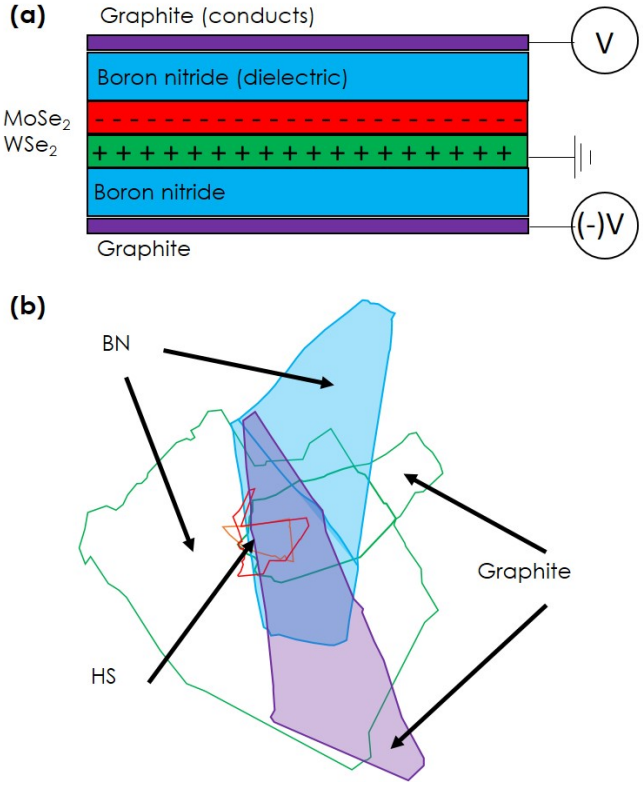

FIG. 3. **(a)** Schematic of how desired electrical control can be achieved in a device. Top and bottom graphite gates can be separately set to fixed potentials without leaking charge through the dielectric h-BN to the HS or shorting to each other. The HS itself is grounded. **(b)** The shape and size of a collection of flakes of various materials and the schematic presented in **(a)** can be combined to arrive at a viable stacking design for a physical device.

C. Transfer

Having established a viable design for achieving the desired electrical control with the material flakes available, the flakes must be precisely stacked. This process, known as the *transfer*, begins with the creation of of a stamp (Figure 4a), which will be used to pick up each flake. The stamp consists of a glass microscope slide covered with a piece of two-sided tape that has a hole punched in the center. Since the stamp will be heated, a small channel should also be cut in the tape so that the

hole-punched center is no longer completely surrounded by tape. This will prevent trapped gas from damaging the stamp when it is heated. The center hole in the tape is filled with a separately prepared dome of polydimethylsiloxane (PDMS). A thin film of polycarbonate (PC) is gently stretched over the PDMS dome and adhered to the two-sided tape. The PC film should be flush with the dome and the tape, but not strained. The PC film provides a sticky surface capable of lifting flakes off of the Si wafer, while the PDMS dome gives compressibility, giving control over how quickly and with what pressure the stamp contacts the Si wafer.

Due to the small size of the flakes and the submicron precision required in the stacking design, the transfer is performed on a *transfer stage*. The stamp is placed sticky-side-down on a micro-manipulator with three translational degrees of freedom. The chip with the flake being picked up is placed on an aluminum block underneath the stamp and held in place by a vacuum chuck running through the center of the block. The block can be moved laterally and rotated; more importantly, it can be heated, which allows for the chip to move vertically due to the thermal expansion of the metal. This degree of freedom, although short-ranged, is perhaps the most important as it is used to gently lift the flake into contact with the stamp after the stamp and chip have been carefully positioned with the mechanical controls. An optical microscope that can be translated and refocused is directed down through the center of the transparent stamp onto the chip, which allows for imaging and careful alignment of the stamp over the chip.

The device is assembled on the transfer stage using a top-down approach and a single stamp. The topmost piece (graphite) is lifted onto the stamp first, and then the chip containing the next piece (h-BN) is substituted for the graphite chip on the transfer stage. The h-BN chip is then rotated and translated until the relative orientation and position between the h-BN flake on the chip and the graphite flake on the stamp match the designed device, and then the stamp is pressed onto the second chip, using the graphite to pick up the h-BN. This process is continued until the device is complete, at which point the stamp is pressed onto the chip and the temperature is raised until the PC melts off. Once this has occurred, the PDMS stamp can be pulled away from the chip, leaving behind a stacked device covered by a layer of PC (Figure 4b). The PC is removed by placing the chip in two successive baths of chloroform for ∼6 hours and ∼30 minutes, respectively, followed by two successive baths of isopropyl alcohol (IPA) for ∼30 minutes and ∼5 minutes, respectively. The chloroform dissolves the remaining PC, and the IPA cleans away any remaining chloroform, which would otherwise evaporate rapidly, potentially leaving behind contaminants on the chip.

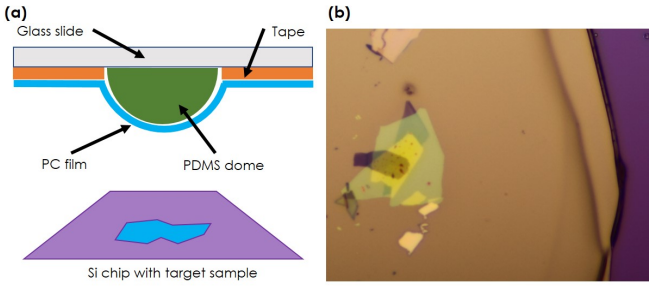

FIG. 4. **(a)** Cross-section schematic showing the stamp, consisting of a glass microscope slide covered by a strong, squishy PDMS dome over which a thin, sticky layer of PC has been pressed flush with the slide and dome, held in place by two-sided tape. A single stamp can pick up layer after layer of material, allowing for top-down assembly of a device. **(b)** Optical microscope image looking down on a stacked device after melting off the PC and device together onto the chip. To the right, the boundary between the remaining PC and the Si chip is visible.

D. Making electrical contact

Having completed the device stacking, the next step in the assembly process is to fabricate electrical contacts to the various flakes in the device. Ultimately, electrical wires need to run from the cryostat mount onto the device itself; however, since wiring directly to the device is impossible, there is an intermediary step in which evaporated gold contacts create a conductive path from the electrical components of the stacked device (top graphite, bottom graphite, and HS) to more separated pads of gold on the chip. These pads provide a larger target for wiring electrical contacts from the outside world to the device.

Creating the gold channels and pads is a four-step, standard electron-beam lithography (EBL) process. First, the entire chip with the stacked device is coated in polymethyl methacrylate (PMMA), a polymer that will serve as the *mask*, or stencil for the gold pattern. Second, an electron beam is used to break bonds in the PMMA, much like an electron jackhammer. Briefly placing the chip in a solvent dissolves the channels etched by the EBL, leaving canals in the PMMA where gold will be allowed to adhere (Figure 5(a,b)). Next, the chip is placed upside-down in an electron-beam evaporator, and a thin film of gold is evaporated onto the surface of the entire chip. In most places, the PMMA coating prevents the gold from contacting the chip surface or the device; however, wherever the EBL process etched away the polymer, gold is evaporated directly onto the surface of the chip and any exposed flakes in the device. Finally, the PMMA is dissolved, washing away the layer of gold covering the device and leaving behind only the desired gold contacts and pads, as shown in Figure 5(c,d).

The final step in fabrication is to connect the gold pads leading to the device to electrical leads in the chip mount. This is achieved using a technique known as wire-

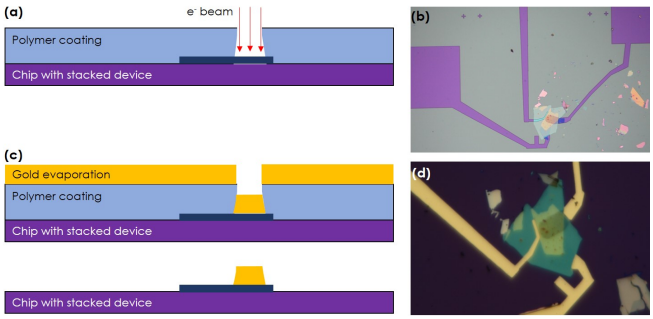

FIG. 5. **(a)** Schematic showing the electron beam etching a path in the PMMA coating. **(b)** Optical microscope image of the pathways (purple) etched in the PMMA mask (gray) covering the chip and device. **(c)** Schematic of gold evaporated onto every exposed surface of the chip and then washed away when the PMMA is dissolved, leaving behind only the gold that evaporated into the canal left by the EBL process. **(d)** Optical microscope image of the gold contacts leading to gold pads left behind after dissolving the remaining PMMA.

bonding, not discussed in great detail here. The chip is secured to a chip mount small enough to fit in the cryostat, and then fine gold wires are individually bonded to connect each gold pad on the chip to a different electrical lead on the chip mount. This step guarantees that the top and bottom gate voltages can be set separately and that the HS can be grounded by controlling the electrical wiring running into the cryostat. At this point, the device is complete and can be sealed inside the cryostat and cooled to a temperature below 4K to minimize thermal noise so that data collection can begin.

III. DATA COLLECTION

Light from a pulsed, 720 nm laser is focused into the cryostat and onto the device. The photon energy associated with these pulses are resonant with the band gap of WSe_2, so electrons in this material are excited to the conduction band and subsequently transferred to the $MoSe_2$ as described in Section I. This charge transfer creates the interlayer excitons, which are the principal interest of this study. Because charge transfer always moves the electrons from the WSe_2 layer to the $MoSe_2$, the excitons form a dipole with fixed dipole moment pointing either parallel or antiparallel to the stacking direction, depending on which layer was picked up first. Thus, if $MoSe_2$ is placed on top of WSe_2, the dipole moment will form pointing down, as shown in the schematic in Figure 3a. Setting gate voltages to equal and opposite values creates a uniform, out-of-plane electric field that can be ramped variably in either direction.

When the interlayer exciton annihilates, the emitted photoluminescence (PL) is collected and collimated with the same objective used to focus the laser onto the sample. The collected PL can then be studied in two important ways. First, a spectrometer is used to resolve photon energies, determining the emission spectrum of the PL. Alternatively, PL can be sent to a single photon counting module, which resolves photon arrival times. By integrating over many PL emission cycles, this approach reveals the decay time of the interlayer exciton state.

IV. RESULTS

As it was not possible to collect data on the device depicted throughout this paper, and since the writing of this paper precedes data collection on a bright and functional replacement device, the data presented here are representative. They have been collected from a device with identical design intended to demonstrate the same effects. There are two results of primary interest to this report: first, resolving the PL spectra as a function of the applied electric field shows the expected quantum-confined Stark shift, in qualitative agreement with Equation 1, reproduced here for convenience.

$$\Delta U = -\boldsymbol{p} \cdot \boldsymbol{E}$$

In Figure 6a, the central red curve shows the baseline PL from interlayer excitons without an electric field present. When the top and bottom graphite gates are held at a fixed potential difference, there is and an electric field and therefore an energy shift in the emission spectra due to the changing exciton energy as governed by Equation 1. A potential difference of V_{top} - V_{bot} = 6V creates an electric field parallel to the exciton dipole moment, which produces a redshift in the emission spectra of $\Delta U \approx -0.025$ eV, seen in the left black curve in Figure 6a. As expected, swapping the sign of the top and bottom gate potentials reverses the effect, producing an electric field antiparallel to the dipole moment, blueshifting the emission spectra by $\Delta U \approx 0.03$ eV (green curve on right in Figure 6a). These electric field-dependent energy shifts of interlayer exciton emission are consistent with a quantum-confined Stark effect.

We can also use these data to approximate the interlayer separation using a simple model. Since the top and bottom gates are set to equal and opposite values of ± 3 V, there is a potential difference of ± 6 V across the bilayer. Approximating the device as a parallel-plate capacitor with an h-BN dielectric of thickness $d = 62$ nm, we can derive an electric field of magnitude $\|\boldsymbol{E}\| = V/d = 9.7 \times 10^7$ V/m. From Figure 6b, we see that parallel alignment of the field and dipole moment produces an energy shift of $\Delta U \approx 0.025$ eV, while antiparallel alignment produces an energy shift of $\Delta U \approx 0.03$ eV. Since the field and dipole moment are always (anti)parallel, Equation 1 reduces to $|\Delta U| = \|\boldsymbol{p}\|\|\boldsymbol{E}\|$, which allows us to compute $\|\boldsymbol{p}\| = |\Delta U|/\|\boldsymbol{E}\|$. With $\|\boldsymbol{p}\| = qd$, where q is the magnitude of the electric charge (in this case the elementary charge e) separated by a distance d, we have $d = \|\boldsymbol{p}\|/e$, which gives an interlayer separation of $a = 2.6$ Å or $a = 3$ Å, depending on whether the energy

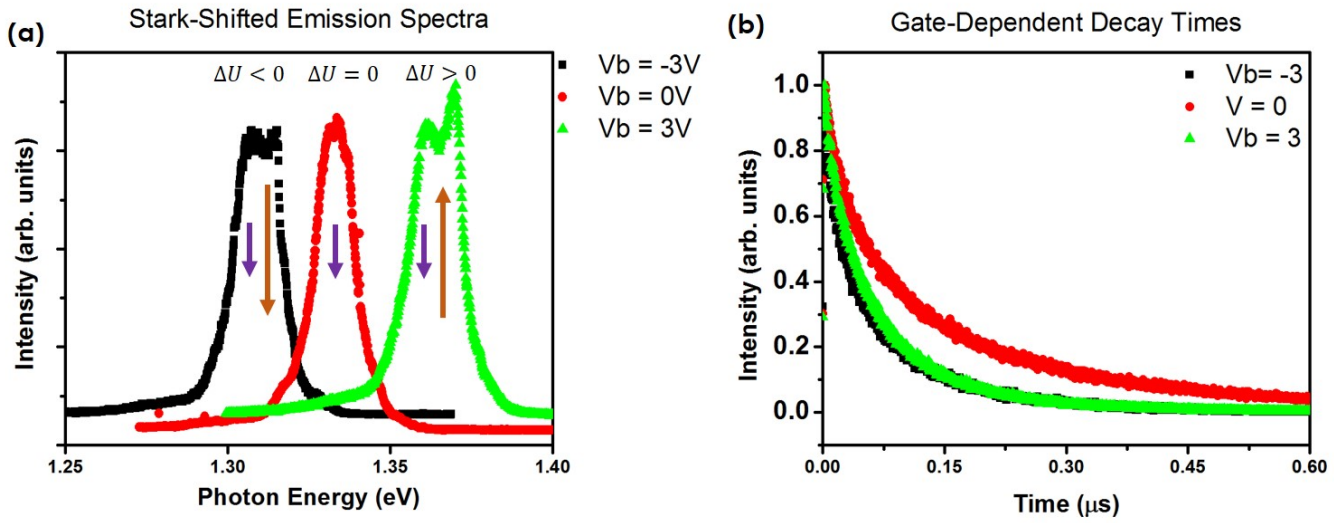

FIG. 6. **(a)** Combination of three separate emission spectra taken with different relative alignments between the dipole moment (purple) and the applied electric field (brown). We note that we see a shift in photon energies as predicted by Equation 1: a field parallel to the dipole moment reduces the dipole energy (black curve), while a field antiparallel to the dipole moment increases the dipole energy (green curve). **(b)** Plot of the exciton decay times associated with the three spectra shown in (a), color coded appropriately. Interestingly, while an applied field produces an asymmetric shift in the photon energies, there is a symmetric effect on the stability of the exciton state, so an external field applied in *either* direction reduces the exciton decay time.

shift for parallel or antiparallel alignment between the dipole moment and the electric field is used. This simple model suggests an interlayer spacing between $MoSe_2$ and WSe_2 that is correct to within a factor of 2.5 with theoretical predictions $a \approx 7$ Å [7, 8]. This approach to computing interlayer spacing, while oversimplified, produces order-of-magnitude estimates consistent with theory. The interlayer spacing could perhaps be more accurately measured if the static dielectric constant of the BN-MX_2-BN heterostructure were better understood.

The decay time of the interlayer exciton in the $MoSe_2$-WSe_2 bilayer decreases when an external electric field is applied. The red curve in Figure 6b shows the decay time when no field is applied. At 0V gate voltage, the 1/e decay time is approximately 100 ns. The black and green curves show a faster ($\sim$ 50 ns) 1/e decay time when a potential difference of $\pm$6V is applied to create an electric field parallel or antiparallel to the dipole moment, respectively. These exciting results require further study to explain the interlayer separation discrepancy and the dependence of the decay time on the field.

V. FUTURE WORK

Two-dimensional physics continues to be a field ripe with opportunities for exciting new discoveries. This report has covered but the tip of the iceberg, discussing only one property of a single type of van der Waals heterostructure, and studying only the dependence of interlayer excitons on the electric field. Future study is required not only to answer the open-ended questions raised by this work (why does an external field decrease the interlayer exciton lifetime?), but to probe the dependence of the properties of a broader variety of van der Waals heterostructures on electric, magnetic, and electromagnetic fields.

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