The Fabrication of Bubble-Free hBN-Encapsulated WTe_2 Devices

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Abstract:

Topological insulators are a relatively new class of material characterized by strong-spin orbit coupling that inverts their band structure and results in conducting edge states that are protected by time reversal symmetry and an insulating band-gap. These materials present a number of possible explorations and applications in the electronics realm. Our lab is currently exploring the properties of WTe_2, a transition metal dichalcogenide with the potential to be a topological insulator in monolayer form. This material poses the most stability and practicality for use; however, due to oxidation, local defects, and other disorders which hinder the study of the material, it must be encapsulated. Our lab uses a fabrication process to produce WTe_2 devices that are encapsulated with hexagonal boron nitride (hBN), an inert, layered dielectric. My work this summer centered on developing a method of clean transfers for fabricating WTe_2 devices. In addition, I fabricated the top and bottom electrostatic graphite gates of the devices with hBN attached to use as an encapsulating layer as well as to allow for tuning the current through the devices. My work will help further the study of WTe_2 as well as other 2D materials.

1. Introduction

The discovery of graphene and other 2D materials with atomic thickness has revealed an abundance of extraordinary electronic properties and functionalities that can be exploited for technological applications.[1] Mechanical and etching techniques along combined with van der Waals (vdW) forces between adjacent layers allows for the fabrication of vertically stacked materials, forming vdW-heterostructured devices.[1] The fabrication of these devices, in conjunction with the discovery of new classes of materials, provides the foundation for unprecedented investigations into nanoscale electronics.

1.1. Topological Insulators

Topological insulators (TIs) are a recently discovered material state in certain compounds of heavy elements that have attracted much recent attention for hosting potentially novel physics as well as application in devices. These TIs are characterized by strong spin-orbit coupling that inverts the electronic band structure, which in turn forces conducting edge states and an insulating bulk as shown in Figure 1 below.[1,2,3] The localized bands on the edge cross at a single point due to this band inversion in the bulk.[2,3] While conducting edge states are possible under certain conditions in other insulating materials, what is unique about the TI edge states is that the

charge carriers are spin-momentum locked by time reversal symmetry, meaning that their spins are locked perpendicular to their direction and they are protected from backscattering.[1,2,3] Especially in 2D materials, the charge carriers experience another phenomenon that proves useful for electronic exploitation: the Quantum Spin Hall Effect (QSHE).[1,2,3]

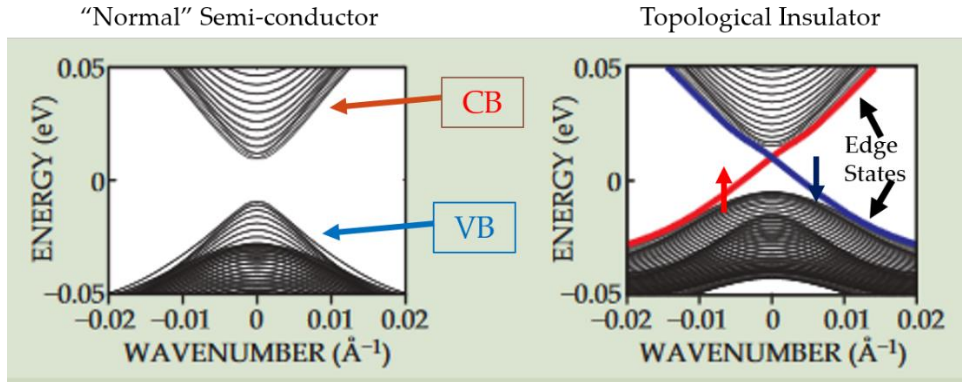
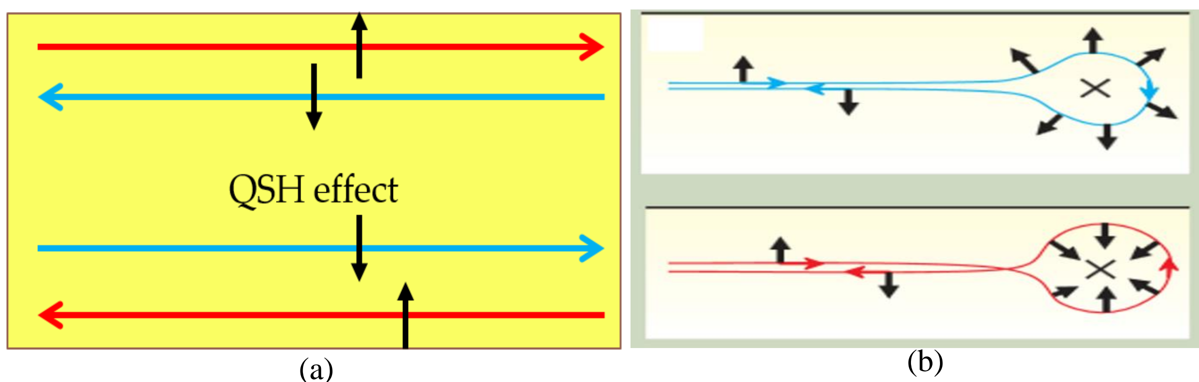


Figure 1. A comparison of the localized band structures of semi-conductors and topological insulators. Notice that the edge states of the TI cross at a single point, as they must due to the band inversion experienced from strong spin-orbit coupling effects.[2]

1.2. Quantum Spin Hall Insulators

The edge states of 2D topological insulators experience partitioning into two lanes of spin-up and spin-down carriers moving in opposite directions (see Fig. 2a below).[2] The carriers can only move in one of two directions due to their spin-momentum locking, and thus if an electron/hole encounters a nonmagnetic impurity, the resulting scattering paths can be either clockwise or counterclockwise.[2] This means that the wavefunctions of the carriers differ in phase by 2π. Thus, the scattering is destructive and strongly discouraged, and perfect transmission of the charge carriers occurs.[1,2]



(a) (b)

Figure 2. (a) A rough illustration of the "traffic lanes" of moving charge carriers with their spins oriented relative to their momenta in the QSH insulator.[2] (b) The two paths a charge carrier can take around a nonmagnetic impurity are clockwise or counterclockwise, differ by a 2π phase, and destructively interfere.[2]

2. Motivations

2.1. Topological Insulator Applications

The electronic properties of these conducting edge states in TIs can be exploited in device fabrication to yield some attractive applications. The existence of exotic particles in quasiparticle form is predicted to occur in TI devices with the addition of other materials. For example, axions, weakly interacting theoretical particles postulated to solve dark matter puzzles, are thought to reside in quasiparticle form in topological magnetic insulators.[2] Majorana fermions, which are their own antiparticle and consequently are considered competent contenders for quantum computing, are predicted to occur in devices made with topological insulators and superconductors due to induced superconductivity via proximity effects.[2] In addition, the vdW devices fabricated using topological insulators, known as Topological Field Effect Transistors (TFETs) could rely on electrostatic gating-induced phase transitions to manipulate the bulk band inversion and thus switch the conducting edge states on or off. This is predicted to allow for much faster electronics in comparison with standard doping and charge carrier depletion used in conventional transistors.[3]

However, potential applications with most current TI candidates face such obstacles as too small of a band-gap for exploiting electronic properties and small signal-to-noise ratios as the result of small numbers of conducting channels.[3] This is potentially remedied with the use of transition metal dichalcogenides.

2.2. Transition Metal Dichalcogenides and WTe_2

Layered transition metal dichalcogenides (TDMCs) are a special class of materials, the most studied of which have chemical formulas MX_2, where generally M = W, Mo and X = Te, Se, S and possess a variety of monolayer polytypes such as 1H, 1T, and 1T'.[3] The 1T' polytypes of these materials hold a high level of promise as effective topological insulators in monolayer form due to the exhibition of strong spin-orbit coupling and large bandgaps compared with most traditional TIs as well as the potential to be topologically insulating at room temperature.[1]

WTe_2, in particular, holds weight as a potential TI candidate due to its relative stability in the 1T' structure compared with other MX_2s.[3] The material has been found to be a semimetal in few layer and monolayer, but application of minor strain of ~1% can lift the gap and create the topological insulating nature.[3] However, WTe_2 presents some potential problems that would seek to hamper its use as an otherwise impressive topological insulator candidate.

2.3. The Necessity of Encapsulation

While WTe_2 is a promising topological insulator, it suffers from rapid oxidation at the surface – the effect of which is clearly most pronounced for few and monolayer samples.[4] In fact, since monolayer WTe_2 will not be functional in a device if it oxidizes, my lab has collected data with a simple trilayer WTe_2 device. As is obvious from a two-terminal resistance measurement for temperature dependence in Figure 3a below, the trilayer device approaches a higher resistance value with temperatures approaching zero, indicative of a semiconductor or insulator. However, if hBN, a layered and inert dielectric that has been shown to favorably insulate MX_2s with no negative impacts on electrical properties[3], is used to encapsulate the device, then the

trilayer device exhibits the behavior as shown in Figure 3b, with resistance decreasing as temperature tends towards zero, indicative of the semimetallic nature of normal WTe_2. While these measurements cannot confirm that it is indeed oxidation that is occurring, they show that the qualitative nature of the device is drastically changed with encapsulation, and that encapsulation preserves the expected behavior. Lee et al has indeed shown that oxidation of the material is indeed what is taking place, and that hBN is indeed an effective insulating layered material.[4]

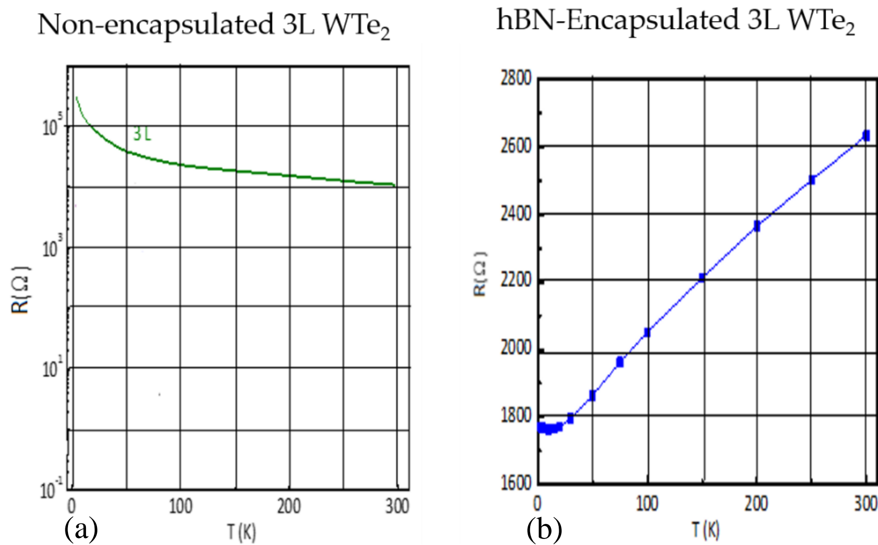


Figure 3. Temperature dependence of resistance of (a) non-encapsulated and (b) hBN-encapsulated trilayer WTe_2 devices. Non-encapsulation displays insulator-like behavior while hBN-encapsulation displays semimetallic behavior.

3. Fabrication of WTe_2 Devices

Our lab therefore fabricates hBN-encapsulated devices based on vdW-TFET designs as shown in Figure 4 below. These devices are built in sequential layers requiring many hours of transferring, patterning and etching. My first job in the process was to fabricate bottom and top graphite gates with hBN used to encapsulate the finished device. All of our fabricated devices involve the use of a special transfer stage setup.

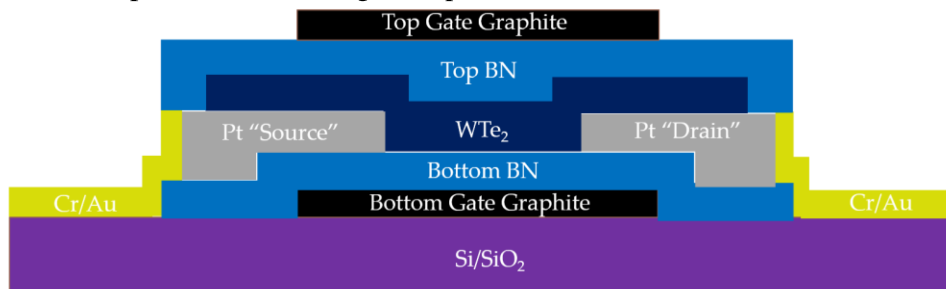


Figure 4. A cross-section schematic detailing the general geometry of the vdW-TFETs fabricated with hBN-encapsulated WTe_2. The small device utilizes wire bonding at the contacts and gates to connect to macroscopic electronics.

3.1. The Transfer Stage Configuration

Figure 5 below highlights our general equipment setup used for the majority of our device fabrication. Our high-power optical microscope allows us to visualize the process and carefully align layers using our specially designed equipment. Central to the transfer process is what we refer to as a "stamp." Stamps are comprised of lumps of an elastomer, polydimethylsiloxane (PDMS), of some geometric shape with a thin polymer film of polycarbonate (PC), stretched across and taped down to a glass slide. These stamps allow us to pick up, layer, and transfer samples from one area to another. The stamps are aligned using a micromanipulator system that allows for micron-scale positioning. Finally, we utilize our own lab-built heating stage with which we can accurately tune the temperature as well as the rate of temperature change. We also exploit the thermal expansion properties of the stage to modify the rate at which our stamps contact the materials. Finally, we use the stage to melt down the PC film when we need the layered materials to remain on the substrate.

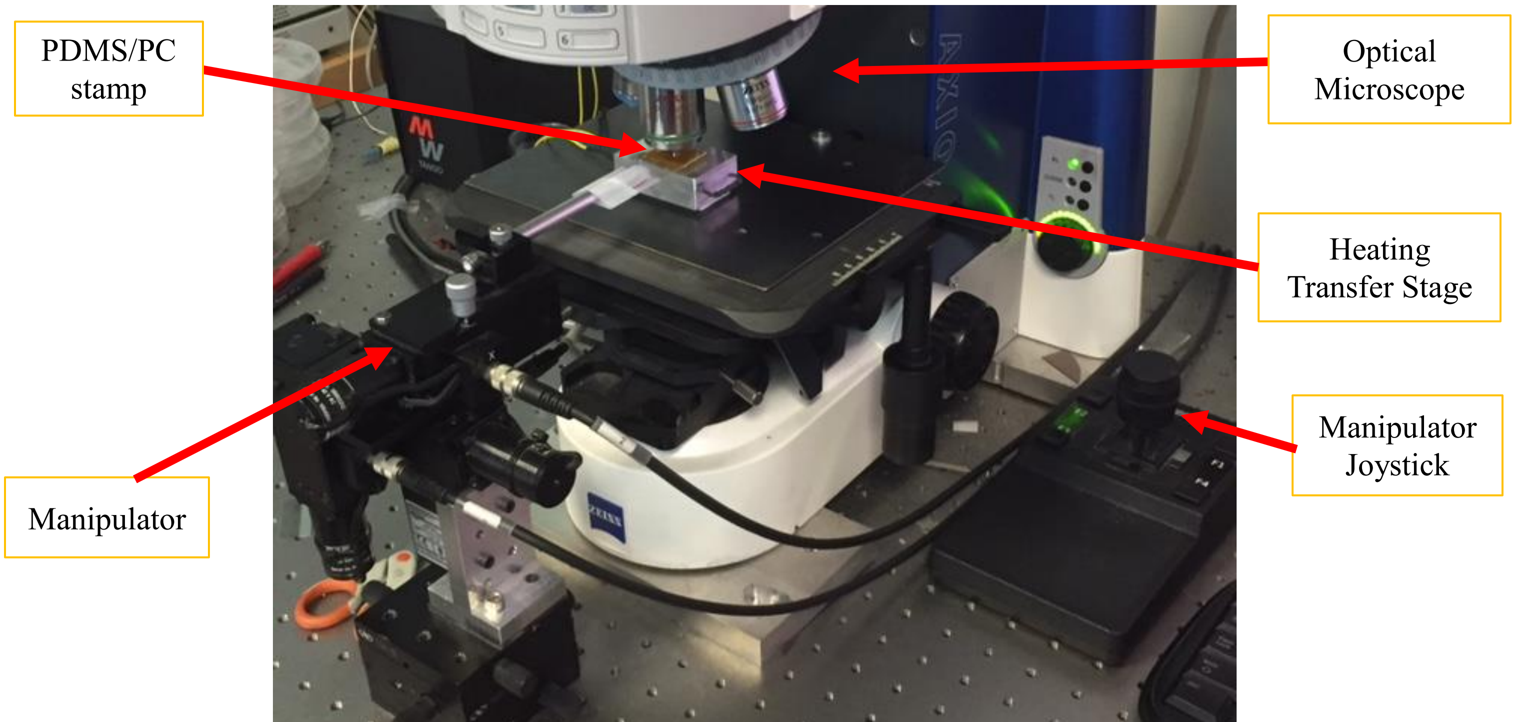


Figure 5. Detail of the transfer setup process. All transfers (besides those that require a vacuum and are performed in a glovebox) are done with this general configuration.

3.2. Finding Suitable Materials for Device Fabrication

We fabricate all devices using a sequential process that involves identification of suitable sample flakes, in-depth imaging for cleanliness, pick-up and transfer to other layers, as well as some additional patterning and etching techniques.

The first category of steps in the fabrication process is that of exfoliating and searching, which is highlighted in the flowchart of Figure 6 below. Since I would be constructing hBN-encapsulating graphite gates, I needed to find suitable flakes of those two materials. This was done using what is known as the "Scotch-tape method" of mechanical exfoliation. The method

relies on placing several large flakes of a bulk material on a piece of tape, ripping it apart several times to separate the flakes, sticking the now exfoliated tape onto a chip of substrate silicon dioxide (SiO_2), and peeling the tape off. Due to van der Waals forces, parts of the flakes will adhere to the substrate and will be sheared from their bulk flakes on the tape.

After exfoliating onto the SiO_2, I take the chip and image it under a high-power optical microscope. The diffraction of light through the flakes at varying thicknesses allows for observation of the nanometer-scale thick materials. Using a 20x resolution, I search through the chip for various suitable flakes of a particular size and geometry for the device. In addition, from previous fabrications, we know roughly the thickness of the flake by its color and can thus use that criterion as well. Once suitable flakes are found, they are then scanned for cleanliness using an Atomic Force Microscope. This process helps us determine if the flakes are usable, since any tape residue or non-uniformity in the layers will introduce conductivity issues later for the completed device. The next steps involve the actual transfer process.

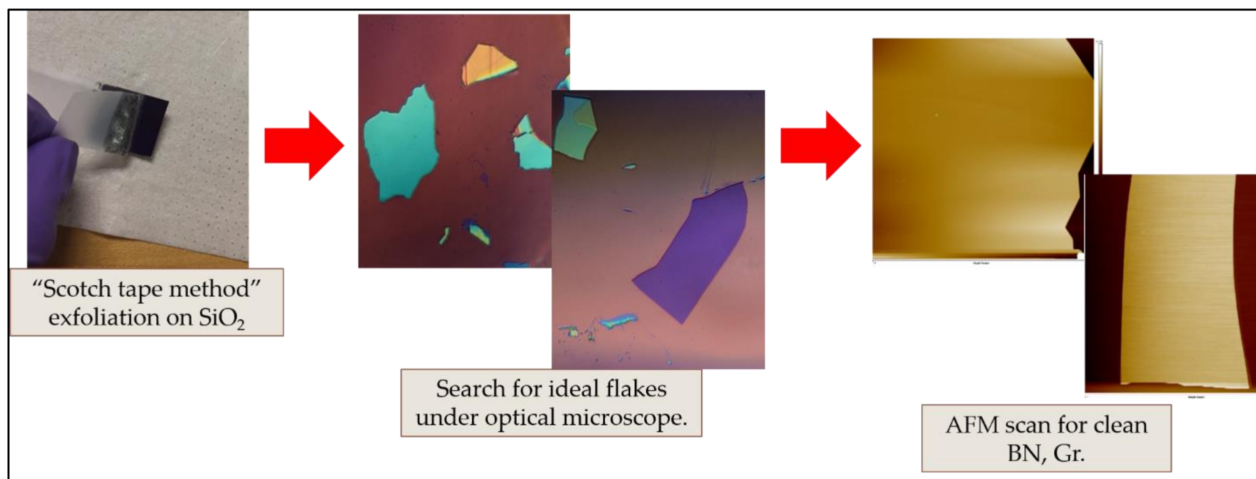


Figure 6. Illustration showing the exfoliation and searching process. The hBN is on the left and the graphite is on the right.

3.3. Pick-Up, Transfer, and Meltdown

After confirming the relative cleanliness of my candidate flakes, the next step is to place the flakes back under the microscope and begin the process of layering them together. Figure below illustrates the flow of the process. First off, I have to place my SiO_2 chip back under the microscope on the heating stage and position a stamp over the flake of hBN. To determine the contact point of the stamp, I use a blank substrate chip to test the location. Next, the temperature of the heating stage is raised to around 110C using an internal heater and the corresponding temperature change measured using an attached thermocouple. Then I slowly lower the stamp down such that the contact point is nearby the candidate flake. The temperature of the stage is slowly increased to 120-130C. This heating causes the stage to expand at a set rate based on the rate of temperature change. Controlling this rate allows for a slow expansion of the stamp's contact point over the flake to improve the efficiency of picking up the flake. After the stamp has made complete contact over the flake, the same process of temperature modulation is performed slowly in reverse and after the contact point passes over the adhered flake, the stamp is slowly removed from contact using the manipulator.

Next, the chip of SiO_2 containing the graphite flake is placed on the stage, and the stamp is positioned over the graphite such that the hBN is aligned according to our needs. After this, once again the stamp is brought down to the point of contact and the heating stage expanded slowly using temperature variation. However, this time, once the contact point of the stamp passes over the aligned layers, the temperature is increased at a rapid rate up to around 170C to melt through the PC and allow the structure to remain on the substrate. Due to van der Waals forces, the graphite will adsorb to the hBN during the process of contacting the stamp, and the layers will become a heterostructure. After the meltdown it becomes necessary to dissolve the melted PC from the substrate.

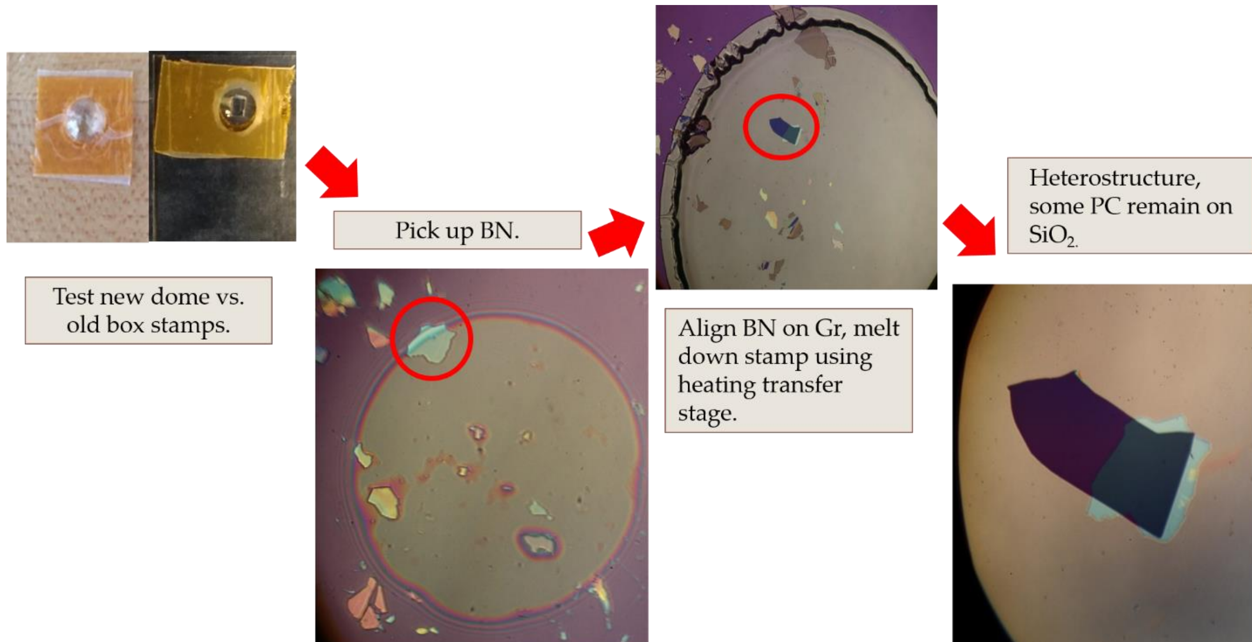


Figure 7. Illustration of the transfer process. Part of the process was testing two different stamp geometries to determine which produces cleaner transfers.

3.4. Cleaning the Gate Heterostructure

Once the PC cools, the chip with the BN-graphite gate must be immersed in a series of alternating baths of chloroform and isopropyl alcohol (IPA) and then cleaned. The chloroform baths dissolve the PC while the subsequent IPA baths help further facilitate the removal of the PC from the surface. Usually, I immersed the chip in an overnight bath of chloroform, followed by a 30-minute bath of IPA, followed by another chloroform bath for several hours, finalized by another 30-minute bath in IPA. Once several of these baths are performed, I placed the chip into an annealing chamber for 2 hours at around 400C to bake in the heterostructure and further remove any PC from the substrate chip. Finally, I scanned the heterostructure for any remaining residue and any potential air bubbles, which we wish to minimize and concerning which I will discuss in more detail further on. Figure 8 below illustrates this final cleaning process.

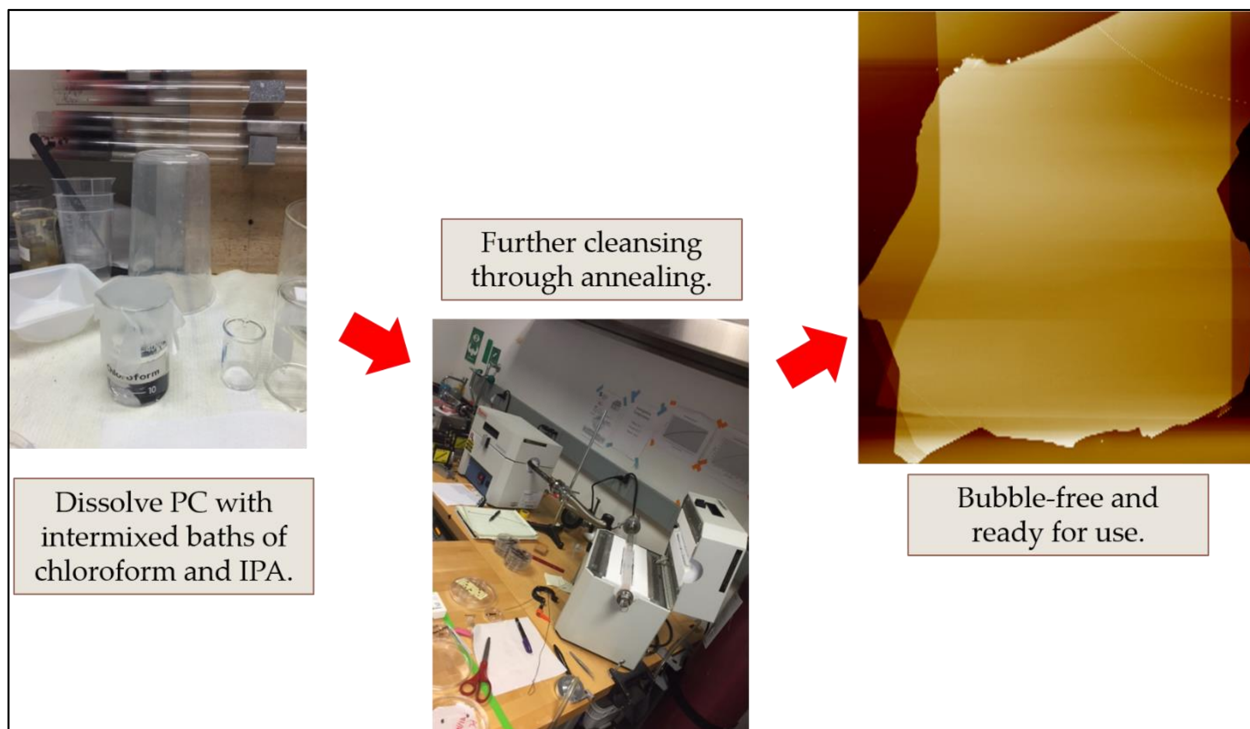


Figure 8. This illustrates the general cleansing process used to clean the gate. The final image is an AFM scan showing the completed heterostructure gate that is free of bubbles and PC residue.

3.5. *Preparing the Rest of the Device*

Other members of my lab utilize a similar procedure to fabricate other layers of the device that involves sandwiching the WTe_2 within the center of the stack. However, they also utilize additional patterning and etching techniques such as electron beam lithography, metal evaporation and deposition, and wire-bonding. These additional techniques allow for the addition of the Pt contacts as well as gold contacts and wires to attach the device to a real electronics system, since the device is so small. A completed WTe_2 device with contacts is shown in Figure 9 below.

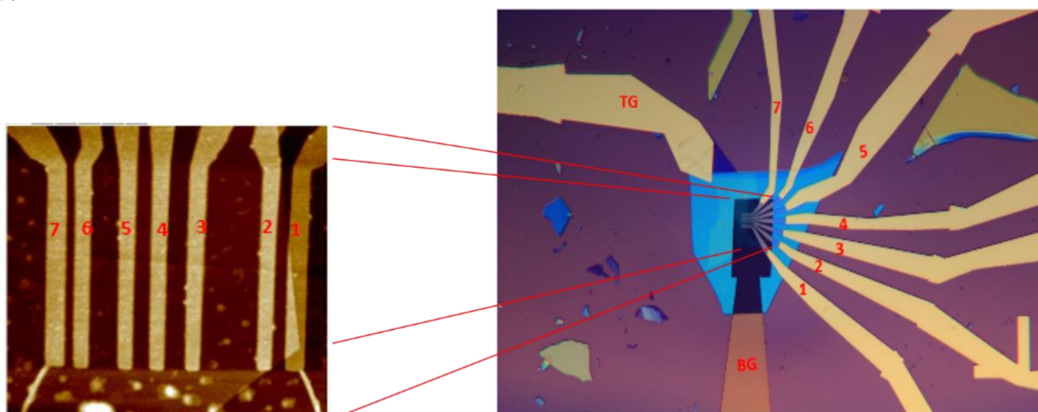


Figure 9. An optical microscope image detailing what a finished hBN-encapsulated WTe_2 device looks like. The zoomed in portion highlights the Pt contacts up close. There are 7 contacts such that a number of different measurements can be made

4. Development of a Bubble-Free Transfer Process

While I was tasked with fabricating these BN-Graphite bottom gates, I was also tasked with developing a method of producing bubble-free transfers. As noted in Figure 7, we utilized two different stamp geometries, a rectangular-box shaped PDMS lump and a dome-shaped PDMS lump. The box stamps have traditionally been used and tend to produce many bubbles. While I did not develop either stamp, I was the sole person tasked with implementing the use of the domed stamps with my gate fabrications. The necessity of bubble-free transfers as well as the development of the domed stamp method I highlight below.

4.1. The Necessity of Bubble-Free Transfers

One of the detriments of the transfer process is that the van der Waals forces between the layers of different materials often facilitate the trapping of air pockets. These so-called “bubbles” cause problems with conductivity by acting as additional dielectrics and disorders in the uniformity of the materials. As such, minimizing these bubbles is of utmost concern. Traditionally, the lab in which I worked utilized a box-shaped PDMS piece in their stamps that tends to result in many bubbles. However, a new domed stamp presents the possibility of cleaner transfers due to the fact that the domes increase the PC tension at the contact point as well as allowing for the transfers to be completed at higher temperatures (110-130C vs 70-90C). We are not quite sure the reasons, but transfers tend to produce fewer bubbles when performed at higher temperatures.

4.2. A Comparison of the Stamp Methods

The transfer mechanism seems to differ between the two different stamp geometries, which may cause a difference in the amount of bubbles formed. With the box stamps, the slow expansion of the contact point over the layers brings the stamp down slowly, hopefully squelching out excess air, but this process is non-uniform. With the domed stamps, I have noticed that the graphite adsorbs to the BN before the contact is actually made on the stamp, and that this only occurs at the higher temperatures and with the smaller contact points of the domed stamps. Perhaps this adsorption forces the air pockets out using capillary action and therefore the bubbles are less likely to occur, but this is purely speculation. Figure 10 below compares the different stamps used as well as the relative cleanliness of completed gates using the different geometries.

Overall, it appears the domed stamps work much better in facilitating bubble-free transfers, and that my work in using them to construct these BN-Graphite gates could be extended to transfers completed for other layers. In light of the prevalence of these bubbles, coupled with the compounding of the detrimental effects throughout various stacked layers, hopefully my development of the use of these domed stamps will transition to the rest of the lab members in future device developments.

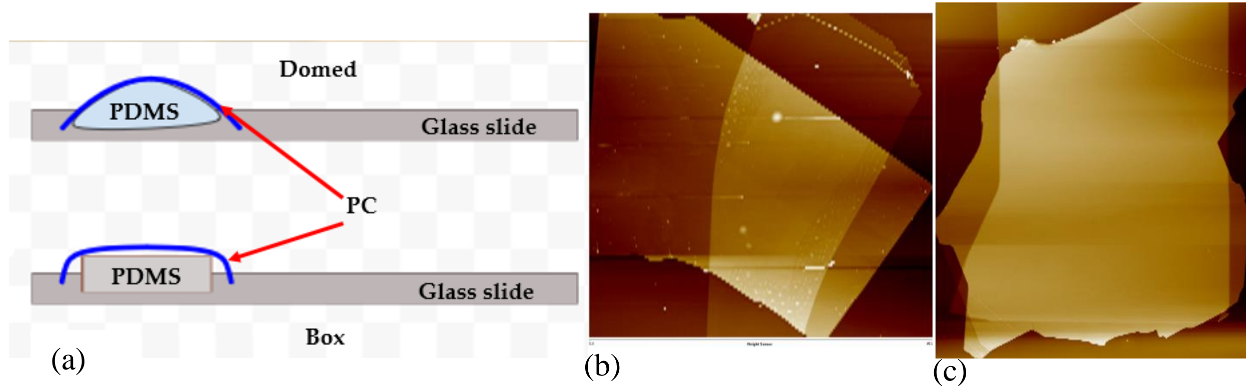


Figure 10. (a) Domed versus boxed PDMS stamp comparison. The contact point as well as PC tension is smaller with the domed stamp due to geometrical differences. (b) A heavily bubbled bottom gate fabricated with a box stamp. (c) A bubble-free bottom gate fabricated using a domed stamp.

5. Conclusions

Overall, WTe_2 is part of a special class of materials known as transition metal dichalcogenides that is predicted to be a topological insulator in 1T' monolayer form under certain conditions. Topological insulators are special materials that, due to strong spin orbit coupling, have inverted valence band structure that results in conducting edge states and insulating band-gaps in the bulk of the material. The unique property of these topological insulators is that these conducting edge states are protected from scattering, thus preserving their perfect transmission, by time reversal symmetry, whereby their momenta must be symmetric upon evolving a state "backwards" in time. These materials also display the Quantum Spin Hall Effect, which further differentiates these conducting edge states by splitting them into two-way "traffic lanes" with spin up carriers moving one way and spin down carriers moving the other way along each edge. Destructive interference from the two different possible paths preserves conduction along the edges.

These topological insulators have many potentially useful applications ranging from quantum computing, axion observations, and electrically written magnetic memory to high speed electronics through topological-FETS, but the material is only stable when properly encapsulated. My lab constructs these TFETs in order to experimentally observe the electronic properties of WTe_2 in few- and mono-layer form. Due to oxidation when exposed to air for large amounts of time, and practical usage of WTe_2 in devices must make use of encapsulation by inert dielectric hexagonal boron nitride, which preserves the semimetallic properties of bulk WTe_2 and allows monolayers of the material to remain intact.

My project was twofold: due to this need of encapsulation as well as the intensive nature of the fabrication process, I helped to fabricate bottom and top graphite gates that were encapsulated with inert dielectric hBN. I was also tasked with developing a method of creating bubble-free transfers using our relatively new domed PDMS/PC elastomer stamps. The bubble-free transfers are crucial to preserving the conductivity and integrity of the devices in measurements. Future works would improve upon my project and utilize what I have developed.

6. Future Works

Currently, my lab is taking measurements with a recently completed bilayer WTe_2 device that allows the possibility for a wide range of potentially rich information about the material. The questions remain as to whether a bilayer of the material will act more like a monolayer (possibly topologically insulating) or whether it will act more like a bulk material (semimetallic). In addition, hopefully the lab will continue to use the hBN-encapsulating gates that I have fabricated for use in further device fabrication to explore the electronic properties of few- and mono-layer WTe_2. Another possible future device would be a Hall bar to measure and compare the experimental differences between few-layer and bulk WTe_2 in terms of magnetoresistance, carrier density of states, and carrier mobility. The lab would use one of the gates that I have created to fabricate such a device.

Finally, the method of bubble-free transfers that I developed using the domed stamps needs to be applied to subsequent layer fabrication in order to produce cleaner and more conductive devices with which to measure. I hope that my work in this area as well as my fabrication of encapsulating gates has proven useful and has paved the way for many potential WTe_2 devices that will help capture the electronic properties of the material for use in novel applications.

7. Acknowledgements

I would like to thank my advisor Prof. David Cobden and his lab, especially Paul Nguyen, Wenjin Zhao, Tauno Palomaki, and Bosong Sun, for their support and involvement in my project. I would also like to extend my gratitude to the University of Washington Institute of Nuclear Theory for nominating and supporting my research experience, and to the National Science Foundation for their sponsorship of this REU through grant PHY-1559631.

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