Fabricating Field Effect Transistors with MX_2

[1]Tanner Pearson,[2]Joe Finney, [2]Zaiyao Fei, and [2]Dave Cobden
[1]Department of Physics and Astronomy, University of South Carolina, Columbia, SC 29225
[2]Department of Physics, University of Washington, Seattle, WA 98195
pearsotg@email.sc.edu

Abstract

The transition metal dichalcogenides are indirect band gap semiconductors that switch to a direct band gap as they approach the limit of a monolayer. This single quality offers much in the way of scientific study since a direct band gap allows for unique optical properties applicable to new age electronics. In addition, they possess a new degree of freedom relevant to the emerging field of valleytronics. Herein, we investigate a fabrication method of novel, ultrathin field effect transistors that utilize these 2-D transition metal dichalcogenides, specifically WSe_2. These devices will allow us to further study the interesting properties of these materials.

I. Introduction

Before the discovery of monolayer graphite, or graphene, many proposed that monolayer materials may exhibit properties uniquely different from their bulk counterparts; however, no such monolayers were proven to exist at the time. When graphene was discovered, the hunt began for monolayers of other materials, which led to the study of the transition metal dichalcogenides. The transition metal dichalcogenides are a group of indirect band gap semiconductors following the formula MX_2 (M=We, Mo, Ti, etc.; X=S, Se, Te). However, as one removes layers from the bulk, the interlayer interactions, which govern the size of the indirect band gap, will decrease, causing the size of the indirect gap to increase. As MX_2 approaches monolayer, the indirect gap becomes larger than the nearby direct band gap, causing MX_2 to switch to a direct gap material (see Figure 1 below) [1].

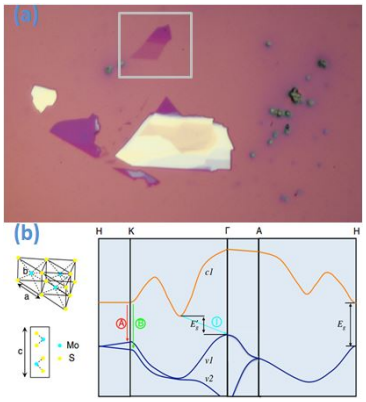

Figure 1: *(a) Optical image of monolayer WSe_2 (outlined) at 100x (b) Lattice structure and band diagram for bulk MoS_2, the latter showing the lowest conduction band and the highest split valence bands. The indirect gap is given by E_g', whereas the direct gap, which takes over at monolayer, is given by E_g [1]*

Monolayer MX_2 is thus much more optically active than bulk MX_2, including increased photoluminescence and absorption [1]. This is because an electron can jump directly across a direct band gap given the absorption or emission of a photon, whereas an electron in an indirect band gap material may only cross a gap when assisted by a phonon. This added necessity to conserve momentum makes the interaction less likely, leading to reduced optical properties. In addition, the staggered hexagonal structure of MX_2 lacks inversion symmetry. This creates a new degree of freedom, the k-valley index, that can be directly manipulated by circularly polarized light and forced to maintain its polarization, in contrast to being submitted to linearly polarized light. This is a quality with major implications in information storage technology and valleytronics [2].

In order to further study the properties of MX_2 materials, we explore methods to fabricate an ultrathin field effect transistor, by which we can observe electronic properties of MX_2 and its viability as a material for modern electronic devices (see Figure 2 for schematic).

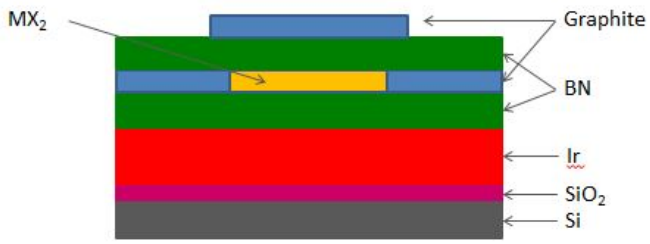

Figure 2: *Schematic of the field effect transistor we fabricate*

Specifically, we use monolayer WSe_2 as our FET channel. For our contacts, as well as our top gate, we use graphite because it is a strong conductor and it need not be evaporated onto the system (where the heating in-

volved in evaporation may cause chemical irregularities between an evaporated material, such as gold, and the other layers of the FET). We then use boron nitride (BN) as top and bottom dielectrics. We choose BN because it is a strong insulator, with and electrical bandgap of approximately 5.97eV, it lacks dangling bonds and surface charge traps, and it has only a 1.7% lattice mismatch with graphite, which will provide for excellent contact between the dielectrics and the contacts [3]. Finally, we use an evaporated iridium backgate and a substrate of SiO_2 atop a Si chip.

II. Methods

We build our FET by first preparing the media on which we can search for the various pieces of our device. It has been seen that silicon wafers coated in a 285nm layer of SiO2 provide the optimal color for finding graphene and other few-layer/monolayer materials [4]. SiO2, however, is often a difficult surface on which to exfoliate, leaving the exfoliated materials thinly spread across the chip. To solve this problem, we first spin coat a layer of polyvinyl acetate (PVA) onto a blank silicon chip. This is a water-soluble layer that is utilized later when removing materials from the chip. After baking, we then spin coat a layer of polymethyl methacrylate (PMMA) on top of the PVA layer. By altering the parameters of spin speed, spin time, and baking temperature, we create PMMA layers that closely resemble the same purple hue of SiO2 and that typically provides a better surface for exfoliation, as seen in Figure 3 below.

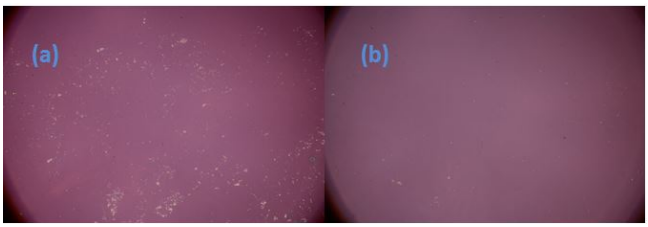

Figure 3: *(a) Exfoliation of BN on PMMA compared to (b) exfoliation of BN on SiO_2.*

We then mechanically exfoliate the material (graphite, BN, or MX2) for which we are searching onto PVA-PMMA coated silicon chips. This is the famous method in which we first set bulk crystals of the material on a strip of scotch tape. Then we snap the tape on and off of itself, cleaving the bulk until it covers all of the space on the tape. We then stick the tape to our surface, press out bubbles with an eraser, and remove the tape [5].

Peeling off the tape leaves a layer of exfoliated crystals on the surface of the PMMA. These flakes can then be sorted through under an optical microscope until we find pieces with the right thickness and smoothness for our device. When we find a candidate, we then image it via AFM, allowing for more detailed surface scans, as seen in Figure 4. The AFM images are critical in that they allow us to see surface imperfections (bumps, folds, etc.) that may have been undetectable optically.

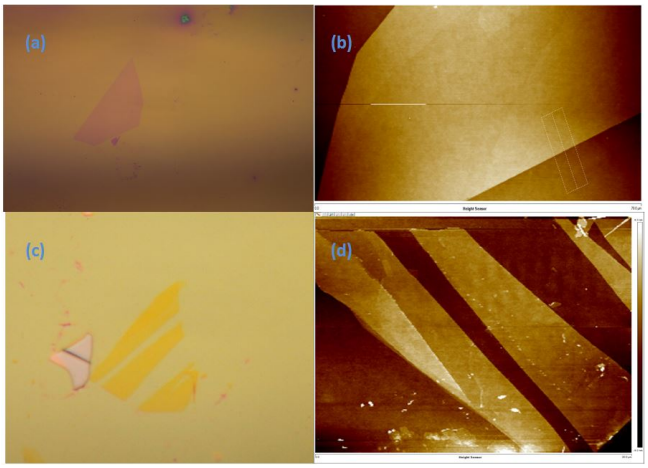

Figure 4: *(a) Optical image of BN at 80x and (b) its corresponding AFM scan. (c) Optical image of two graphite contacts at 80x and (d) its corresponding AFM scan. The AFM scan shows that the graphite had both a step and several bumps unseen in the optical image*

For graphite, we look for pieces that are roughly 5-15nm thick. We do not want to use flakes that are too thin, particularly monolayers, in order to avoid introducing the abnormal properties of graphene into our device. Due to the geometry of the device, we also do not want to use very thick pieces that will not conform well to the rest of the layers (although the top gate may be thicker as it will have nothing placed on top of it). We search for BN pieces that are 8-15nm. Again, the lower limit is chosen to prevent the tunneling of electrons through the dielectric (hence leaking of the FET), and the upper limit so as to maintain the proper screening of the Schottky barriers that form at the interface between the graphite contacts and MX_2 channel.

After all the pieces of our device have been assembled, we then go through a series of transfers in order to stack the pieces on top of each other. All of our pieces are found on PMMA; however, we want our final device on SiO_2 (on which we have already evaporated our Ir backgate). We do this with "wet" transfers (Figure 5 below). In this process, we float the PMMA-coated chip with a desired piece in water and allow the water-soluble PVA to dissolve, leaving the PMMA film with our piece floating at the top of the water. We can then pick this flake up with a wire loop and let dry. Then we place the loop on a micromanipulator and, while

viewing under a microscope, line up and place the piece in a specific location on a SiO_2 chip. The PMMA will stick down when pressed to the surface, and we cut around the outside of the PMMA in order to remove the loop while leaving the piece on the chip. Excess PMMA can then be removed in an acetone bath.

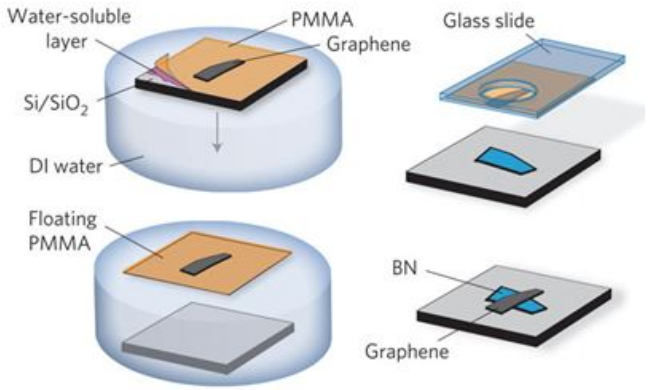

Figure 5: *Step-by-step diagram of the wet transfer method (Note: we typically use a wire loop to pick up the floating PMMA as opposed to a glass slide) [3]*

In order to transfer pieces on top of each other, we then utilize a "dry" transfer method that is based entirely on the van der Waals attractions between corresponding surfaces (see Figure 6). First we spin coat a layer of poly-propylene carbonate (PPC) on top of poly-dimethyl siloxane (PDMS), the latter of which acts as a transparent elastomer stamp. We then pick one piece up off of SiO_2 by stamping the PPC onto the surface. When heated to a certain temperature (roughly 40°C), the van der Waals forces are stronger between the PPC and the given flake than they are between said flake and SiO_2 . Thus, the piece will lift up, and then the same method can be used to stack multiple pieces on top of one another. The stack can then be deposited by heating the SiO_2 chip to approximately 90°C, and the excess PPC can be removed in a DCM bath.

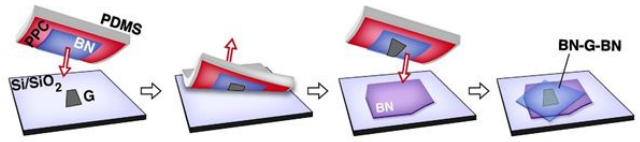

Figure 6: *Step-by-step diagram of the dry transfer method. Depicted here is the assembly of a BN/graphite heterostructure, but we modify the method for our FET [6]*

III. Results and Discussion

In Figure 7 is an optical image of a finished FET with a corresponding AFM scan of the WSe_2 channel spread over the two graphite contacts. While the device may look fine optically, one can see several issues in the AFM image. First, the white lines cutting across the image represent folds in the device. By taking AFM scans after each transfer, we know that the folds arrived after the top BN layer was dry transferred, meaning the folds must be in the top dielectric. Furthermore, the outlined region in the bottom portion of the figure shows an area of the device that looks as if it was etched through (which did not exist before the BN transfer). This was the ultimate downfall of device, since the apparent tearing broke the connection between the channel and contacts. Unfortunately, the reason for this tearing is not understood.

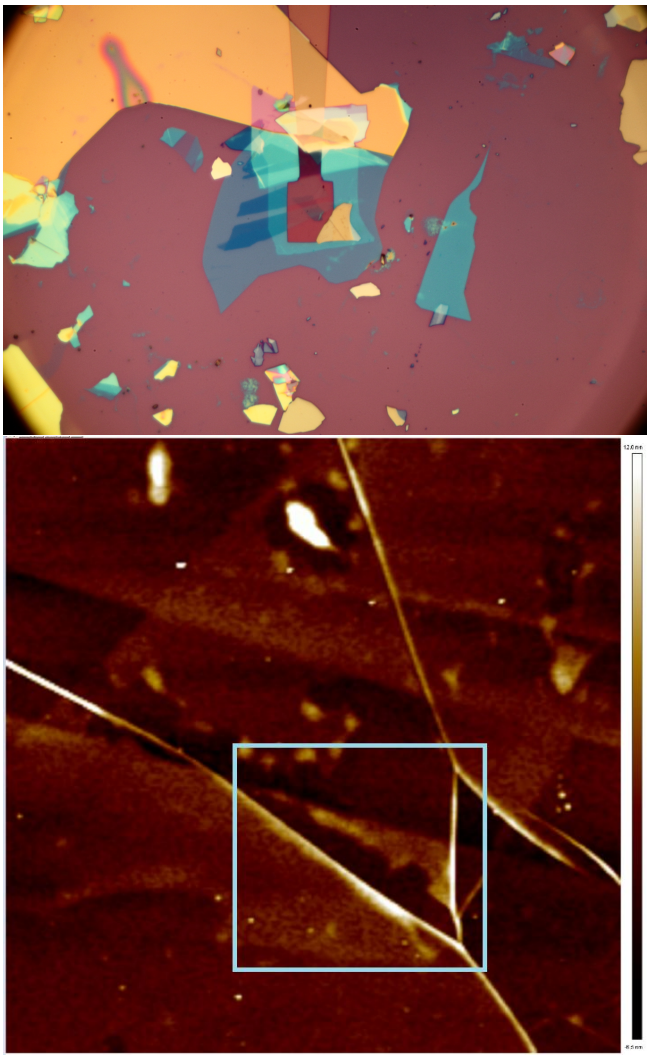

Figure 7: *Optical image of a completed FET (top); 8µm AFM scan of the device, centered on the WSe_2 channel with apparent tearing outlined (bottom)*

Evidently, we still have a need for improved transfer techniques. Our wet transfer method is relatively clean, leaving little residue, but it lacks the accuracy needed to

stack successive pieces and it takes a significant amount of time to complete due to the drying process. Dry transfer, on the other hand, is relatively quick and it is much easier to align; however, it has provided many issues with folding and tearing of pieces during the transfer process, which effectively ruins a device. While we have made some progress with our current techniques, the results are still variable. Moreover, while many of our failures are related to human error, some are more difficult to explain even when we have proceeded carefully (as in the case of the device described above).

IV. Future Work

Within the next few months, much work will go into improving our device fabrication methods. In particular, we will explore a new transfer method that uses polycarbonate (PC) spun onto PDMS in tandem with van der Waals forces between pieces of the FET to create a stack that can be transferred as one. In addition, there is an ongoing effort to grow MX_2 via chemical vapor deposition. Success in that project will greatly decrease the time needed to create a device, since MX_2 monolayers are exfoliate sparsely and are notoriously difficult to search for.

Once we create a working FET, we can investigate the various electronic properties of the device, including carrier mobility and on/off ratio. These are interesting from an engineering standpoint and will allow us to understand the viability of our device in the world of modern electronics.

Lastly, a long-term goal is to use the four terminals of our FET (top and bottom gates along with the two contacts) to explore different Hall effects in WSe_2. Particularly, we are interested in the quantum spin Hall effect, which is a localized effect in 2D electron gases (hence, our 2D MX_2 monolayer). In order to see this effect, we must operate the FET in a cryostat because low temperatures will be needed to reduce thermal excitations in the WSe_2 electrons, keeping them in a constant location. Additionally, the benefit of our FET is that it will allow us to specify the number of charge carriers in the WSe_2 channel by adjusting the gate voltages, providing us an easily manipulated variable.

V. Acknowledgements

I would like to thank Dr. Dave Cobden for hosting and advising me throughout this summer, as well as Joe Finney, Paul Nguyen, and Zaiyao Fei for the day-to-day support they offered me in the lab. I also thank Gray Rybka, Alejandro Garcia, Subhadeep Gupta, Janine Nemerever, and Linda Vilett for organizing the INT REU and making it a great all-around experience. Funding for this project was provided by the NSF.

References

[1] Mak, K.F., Lee, C., Hone, J., Shan, J., Heinz, T.F. "Atomically Thin MoS_2: A New Direct-Gap Semiconductor." *Physical Review Letters* 105, 136805 (2010).

[2] Xu, X., Yao, W., Xiao, D., Heinz, T.F. "Spin and pseudospins in layered transition metal dichalcogenides." *Nature Physics* 10, 343-350 (2014).

[3] Dean, C. R., A. F. Young, I. Meric, C. Lee, L. Wang, S. Sorgenfrei, K. Watanabe, T. Taniguchi, P. Kim, K. L. Shepard, and J. Hone. "Boron Nitride Substrates for High-quality Graphene Electronics." *Nature Nanotechnology* 5.10 (2010): 722-26.

[4] Blake, P., E. W. Hill, A. H. Castro Neto, K. S. Novoselov, D. Jiang, R. Yang, T. J. Booth, and A. K. Geim. "Making Graphene Visible." *Applied Physics Letters* 91.6 (2007): 063124.

[5] Novoselov, K. S., and A. H Castro Neto. "Two-dimensional crystals-based heterostructures: materials with tailored properties." *Physica Scripta* T146 (2012): 014006.

[6] Wang, L., I. Meric, P. Y. Huang, Q. Gao, Y. Gao, H. Tran, T. Taniguchi, K. Watanabe, L. M. Campos, D. A. Muller, J. Guo, P. Kim, J. Hone, K. L. Shepard, and C. R. Dean."One-dimensional electrical contact to a two-dimensional material." *Science* 342.6158 (2013): 614-17.